LINEAR

Integrated Circuit Databook

PLESSEY
SEMICONDUCTORS

Linear integrated circuits

PLESSEY
SEMICONDUCTORS

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MATCHED NPN TRANSISTORS & ARRAYS

RADIO COMMUNICATIONS CIRCUITS

quality assurance

Plessey Semiconductors' quality policy is Total Quality Control by involvement in :–

Receiving Inspection
Process Control for Mask Making
Process Control for Slice Processing
Process Control of Assembly
Process Control of Electrical Testing
Package Evaluations
Process Assessments

Each stage of IC manufacture is audited by the QA department (which is independent of the manufacturing unit). Each operation and process control procedure is fully documented.
Typical electrical test is a 100% operation, which is carried out by production. QA perform a process control on the operation, where devices are sampled using the double sampling plan with an effective AQL of 0.65% and LTPD of 10%.
This enables Plessey Semiconductors to offer :–

a) Factory Approval
   to **BS9300** for semiconductor devices of Assessed Quality (BSI Certificate 1053/M)
   to **BS9400** for integrated circuits of Assessed Quality (BSI Certificate 1053/M)
   to **CECC 50000** Inspection Organisation to document level 1 (BS9300). M0020/CECC refers
   to **DEF STAN 05-21** QC System requirements for Industry (Equivalent to AQAP-1) Certificate 65752/1/01 refers.
b) Additional Release Conditions
   to **6/49** Defence Quality Assurance Board Certificate (DQAB 38020)
   to **MOD (N)** Navy Department Inspection Authority
   Private Sales Plessey's own Certificate of Conformance.

Devices are also manufactured, tested and supplied to MIL-STD-833 – the US Military Standard; Test Methods and Procedures for Microcircuits, and MIL-M-38510 – US Military Specification, Microelectronics; General Specifications for.

technical data

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL301K SL301L
DUAL NPN TRANSISTORS

The SL301K and SL301L are dual NPN transistors manufactured as monolithic integrated circuits. Their close parameter matching and thermal tracking are considerably better than conventional 'two chip' duals; the frequency response is equally superior.

The SL301K and L have identical electrical specifications but differ in packaging. The SL301 is pin compatible with existing SL300 series products and available in both metal can (CM) and ceramic dual-in-line (DG) packages. The SL301K is available only in metal can (CM) and is pinned to be compatible with conventional discrete 'two chip' products. Note, however, that an extra connection is required to allow the substrate to be connected to the most negative part of the circuit.

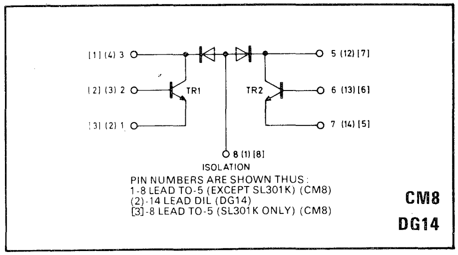


Fig. 1 SL301 circuit diagram

ORDERING CODES:

SL301K - CM
SL301L - CM
SL301L - DG

QUICK REFERENCE DATA

- Max voltage 12V to 20V
- Operating temperature range −55°C to +175°C

VOLTAGE RATING

The maximum voltage allowed between collector and emitter of each transistor is limited by dissipation and voltage breakdown. Assuming dissipation is low the rating may be determined from the following details:

(a) Forward bias condition

If the transistor is conducting the maximum collector-emitter voltage allowable is at least equal to V_{CEO} (12V). In cases where the collector current does not exceed 5mA and a resistor R is connected between base and emitter the V_{CER} rating may be determined from Fig. 8; this voltage lies between 12V and 20V depending on the value of R.

(b) Unbiased condition

If the transistor is operated with no connection to the base the maximum safe collector-emitter voltage is V_{CEO} (12V). In cases where the base emitter voltage has been reduced so the transistor is conducting at a low level it is generally permissible to increase this towards V_{CBO} (20V).

(c) Reverse biased condition

If the base of the transistor is connected via the resistor to a supply voltage equal to, or more negative than, the emitter voltage the maximum collector-emitter voltage V_{CEX} allowable (assuming negligible collector current) is limited by V_{CBO} (20V). For example, if the base is at −5V with respect to the emitter, the maximum collector voltage will be +15V.

FEATURES

- Close V_{BE} Matching
- High Gain
- Good Frequency Response
- Excellent Thermal Tracking

APPLICATIONS

- Differential Amplifier
- Comparator
- Stable Current Source

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors: thermal ratings apply to total package dissipation.

The isolation pin must always be negative with respect to the collectors.

No one transistor may dissipate more than 75% of the total power.

Storage temperature	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance:	
TO-5 (CM)	250°C/W
Ceramic DIL	106°C/W
Chip-to-case thermal resistance:	
TO-5 (CM)	80°C/W
Ceramic DIL (DG)	39°C/W
V_{CBO}	20V
V_{CEO}	12V
V_{CER}	12V to 20V (see graph)
V_{EBO}	5V
V_{CIO}	25V
I_{CM}	50mA

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
$T_{amb} = +25°C$

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Each Transistor					
BV_{CBO}	20			V	$I_C = 10\ \mu A$
BV_{CEO}	12			V	$I_C = 5mA$
BV_{EBO}	5			V	$I_E = 10\ \mu A$
BV_{CIO}	25			V	$I_C = 10\ \mu A$
h_{FE}	30	50			$V_{CE} = 5V, I_C = 10\ \mu A$
	40	70			$V_{CE} = 5V, I_C = 100\ \mu A$
	60	100			$V_{CE} = 5V, I_C = 1mA$
	50	80			$V_{CE} = 5V, I_C = 10mA$
$V_{CE\ (SAT)}$		0.36	0.6	V	$I_C = 10mA, I_B = 1mA$
$V_{BE\ (SAT)}$	0.7	0.8	0.9	V	$I_C = 10mA, I_B = 1mA$
I_{CBO}			10	nA	$V_{CB} = 10V$
I_{EBO}			10	nA	$V_{EB} = 2V$
I_{CIO}			10	nA	$V_{CI} = 10V$
C_{OB}			2	pF	$V_{CB} = 5V$
C_{IB}			4	pF	$V_{BE} = 0v$
C_{CI}			6	pF	$V_{CI} = 5V$
f_T	400	680		MHz	$V_{CE} = 5V, I_C = 5mA$
Matching					
h_{FE1}/h_{FE2}	0.9		1.1		$V_{CE} = 5V, I_C = 100\ \mu A$
	0.9		1.1		$V_{CE} = 5V, I_C = 1mA$
ΔV_{BE}			3	mV	$V_{CE} = 5V, I_C = 100\ \mu A$
			3	mV	$V_{CE} = 5V, I_C = 1mA$
$\frac{\partial \Delta V_{BE}}{\partial T_{amb}}$			10	μV/°C	$V_{CE} = 5V, I_C = 100\ \mu A$

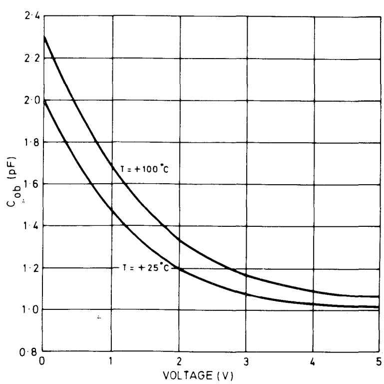


Fig. 2 Output capacitance (C_{ob}) v. voltage

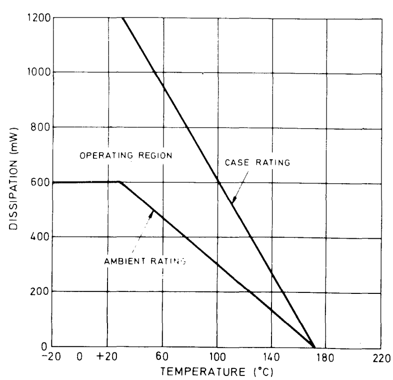


Fig. 3 Power dissipation derating curves (TO-5 package)

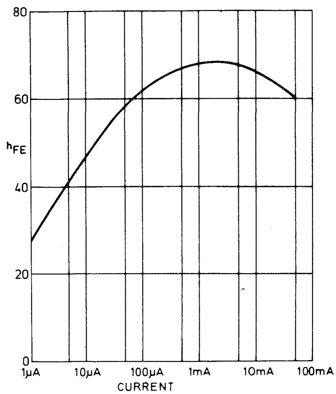


Fig. 4 Typical variation of h_{FE} with collector current

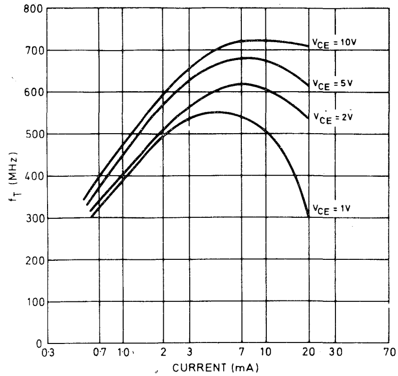


Fig. 5 f_T v. collector current ($f_T = f|h_{fe}|$. $f = 100$ MHz)

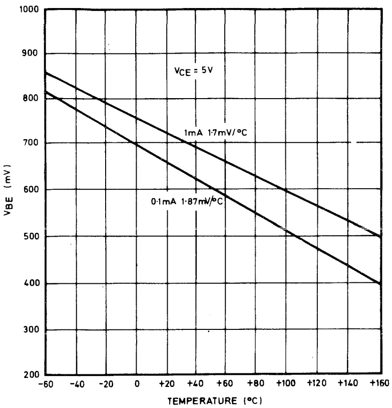


Fig. 6 V_{BE} v. temperature

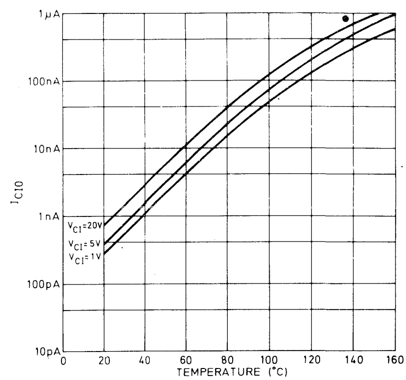


Fig. 7 Typical I_{CIO} v. temperature

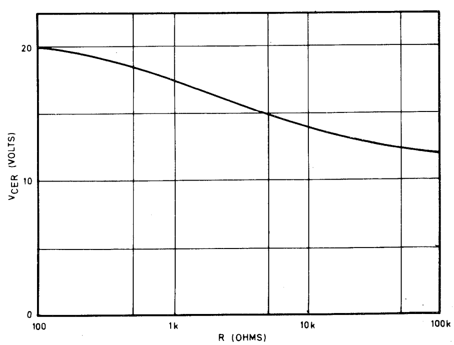


Fig. 8 Relationship between V_{CER} and R_{BE}

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL303L
TRIPLE NPN TRANSISTORS

The SL303 is a silicon monolithic integrated circuit comprising three separate transistors, two of which have closely matched parameters ; the third transistor may be used as, for example, a tail transistor. The SL303 devices are available in 10-lead TO—5 (CM) and 14-lead dual-in-line (DG) packages.

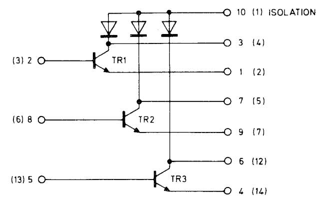


Fig. 1 Circuit diagram

ORDERING CODES:

SL303L — CM

SL303L — DG

FEATURES

- Close V_{BE} Matching
- High Gain
- Good Frequency Response
- Excellent Thermal Tracking

APPLICATIONS

- Differential Amplifier
- Comparator

VOLTAGE RATING

The maximum voltage allowed between collector and emitter of each transistor is limited by dissipation and voltage breakdown. Assuming dissipation is low the rating may be determined from the following details:

(a) Forward bias condition

If the transistor is conducting the maximum collector-emitter voltage allowable is at least equal to V_{CEO} (12V). In cases where the collector current does not exceed 5mA and a resistor R is connected between base and emitter the V_{CER} rating may be determined from Fig. 8 ; this voltage lies between 12V and 20V depending on the value of R.

(b) Unbiased condition

If the transistor is operated with no connection to the base the maximum safe collector-emitter voltage is V_{CEO} (12V). In cases where the base emitter voltage has been reduced so the transistor is conducting at a low level it is generally permissible to increase this towards V_{CBO} (20V).

(c) Reverse biased condition

If the base of the transistor is connected via the resistor to a supply voltage equal to, or more negative than, the emitter voltage the maximum collector-emitter voltage V_{CEX} allowable (assuming negligible collector current) is limited by V_{CBO} (20V). For example, if the base is at —5V with respect to the emitter, the maximum collector voltage will be +15V.

QUICK REFERENCE DATA

- Max voltage — 12V to 20V
- Operating temperature range — −55°C to +175°C

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors: thermal ratings apply to total package dissipation.

The isolation pin must always be negative with respect to the collectors.

No one transistor may dissipate more than 75% of the total power.

Storage temperature	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance:	
TO-5 (CM)	250°C/W
Ceramic DIL	106°C/W
Chip-to-case thermal resistance:	
TO-5 (CM)	80°C/W
Ceramic DIL (DG)	39°C/W
V_{CBO}	20V
V_{CEO}	12V
V_{CER}	12V to 20V (see graph)
V_{EBO}	5V
V_{CIO}	25V
I_{CM}	50mA

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Each Transistor					
BV_{CBO}	20			V	I_C = 10 μA
BV_{CEO}	12			V	I_C = 5mA
BV_{EBO}	5			V	I_E = 10 μA
BV_{CIO}	25			V	I_C = 10 μA
h_{FE}	30	50			V_{CE} = 5V, I_C = 10 μA
	40	70			V_{CE} = 5V, I_C = 100 μA
	60	100			V_{CE} = 5V, I_C = 1mA
	50	80			V_{CE} = 5V, I_C = 10mA
$V_{CE\ (SAT)}$		0.36	0.6	V	I_C = 10mA, I_B = 1mA
$V_{BE\ (SAT)}$	0.7	0.8	0.9	V	I_C = 10mA, I_B = 1mA
I_{CBO}			10	nA	V_{CB} = 10V
I_{EBO}			10	nA	V_{EB} = 2V
I_{CIO}			10	nA	V_{CI} = 10V
C_{OB}			2	pF	V_{CB} = 5V
C_{IB}			4	pF	V_{BE} = Ov
C_{CI}			6	pF	V_{CI} = 5V
f_T	400	680		MHz	V_{CE} = 5V, I_C = 5mA
Matching(TR1, TR2 only)					
h_{FE1}/h_{FE2}	0.9		1.1		V_{CE} = 5V, I_C = 100 μA
	0.9		1.1		V_{CE} = 5V, I_C = 1mA
ΔV_{BE}			3	mV	V_{CE} = 5V, I_C = 100 μA
			3	mV	V_{CE} = 5V, I_C = 1mA
$\frac{\partial \Delta V_{BE}}{\partial T_{amb}}$			10	μV/°C	V_{CE} = 5V, I_C = 100 μA

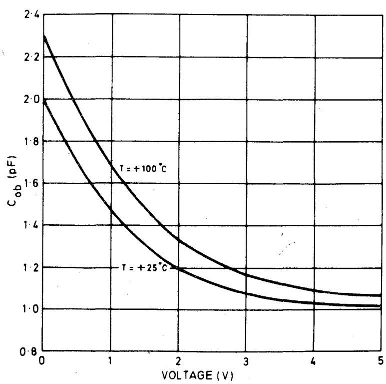


Fig. 2 Output capacitance (C_{ob}) v. voltage

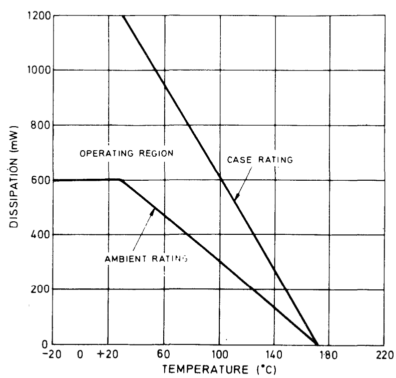


Fig. 3 Power dissipation derating curves (TO-5 package)

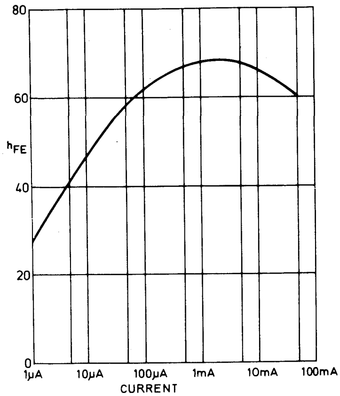


Fig. 4 Typical variation of h_{FE} with collector current

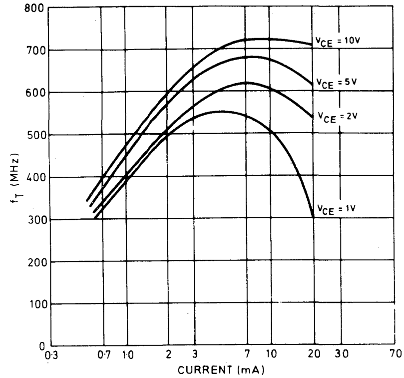


Fig. 5 f_T v. collector current ($f_T = f|h_{fe}|$. $f = 100$ MHz)

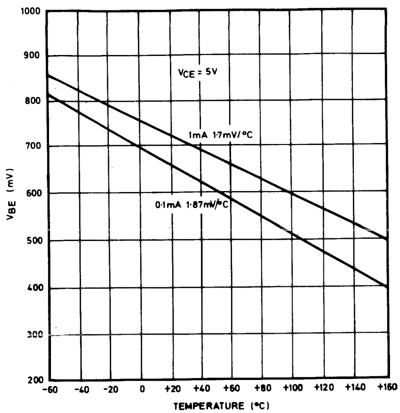


Fig. 6 V_{BE} v. temperature

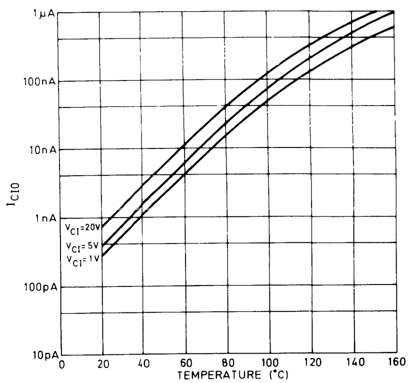


Fig. 7 Typical I_{CIO} v. temperature

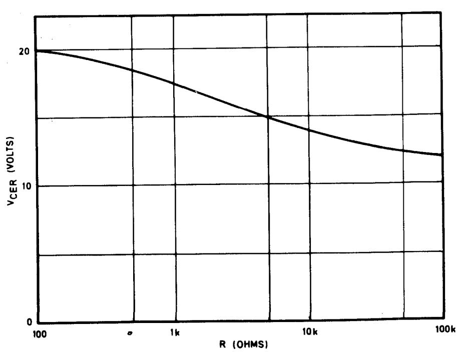


Fig. 8 Relationship between V_{CER} and R_{BE}

PLESSEY
SEMICONDUCTORS

MODULATOR DEMODULATOR

SL355C TBA673C

4-TRANSISTOR MODULATOR/DEMODULATOR

The TBA673 and SL355 are monolithic integrated 4-transistor modulator/demodulator circuits. Featuring close similarity in the characteristics of the individual transistors and optimal tracking of parameters with temperature, these devices give better balancing (and therefore less carrier leakage) than discrete circuits. The use of transistors instead of the more conventional diodes results in an improved isolation between input and output circuits.

The choice between TBA673 and SL355 will depend largely on the application. For example, the TBA673 has higher voltage characteristics than the SL355, but the SL355 would be used where high frequency performance is the prime consideration.

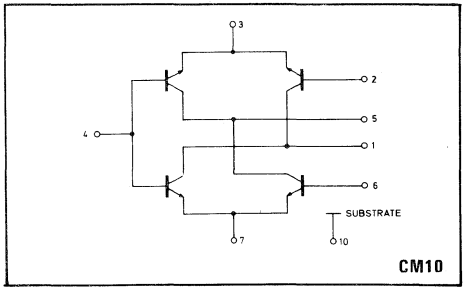


Fig. 1 Circuit diagram

FEATURES

- ΔV_{BE} = ±5mV Max.
- Close h_{FE} Matching
- High f_T : 250 MHz (TBA673)
  600 MHz (SL355)

APPLICATIONS

- DSB/DSBSC/AM Modulation
- Synchronous Detection
- FM Detection
- Choppers
- Signal Routeing
- Telephone Transmission (TBA673)

ABSOLUTE MAXIMUM RATINGS

Electrical (Each Transistor)

Rating	Symbol	TBA673	SL355	Units
Collector-emitter voltage	V_{CEO}	45	12	V
Collector base voltage	V_{CBO}	80	20	V
Emitter-base voltage	V_{EBO}	7.2	5	V
Collector-isolation voltage	V_{CI}	80	25	V
Collector current	I_C	100	20	mA

Power

Total power dissipation: See Fig. 3

Temperature

Storage temperature, T_{stg}: –35° to +125°C
Operating temperature, T_{amb}: See Fig. 3

NOTE
The substrate pin must be more negative than each of the collectors.

ELECTRICAL CHARACTERISTICS – TBA673

Test conditions (unless otherwise stated):

T_{amb} = +25°C

Characteristics apply to each transistor

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Condition
Each transistor						
Collector-base breakdown voltage	BV_{CBO}	80			V	I_C = 10μA, I_E = 0
Collector-emitter sustaining voltage	LV_{CEO}	45			V	I_C = 5mA, I_B = 0
Emitter-base breakdown voltage	BV_{EBO}	7.2		8.0	V	I_E = 10μA, I_C = 0
Collector-isolation breakdown voltage	BV_{CIO}	80			V	I_C = 10μA
Collector-base leakage current	I_{CBO}			10	nA	V_{CB} = 10V, I_E = 0
Emitter-base leakage current	I_{EBO}			1	nA	V_{EB} = 2V, I_C = 0
Collector-isolation leakage current	I_{CIO}			3	nA	V_{CI} = 10V
Large signal current transfer ratio	h_{FE}	80		300		I_C = 5mA, V_{CE} = 5.0V
Transition frequency	f_T	250			MHz	I_C = 5mA, V_{CE} = 5.0V
Collector-isolation capacitance	C_{CI}			6.5	pF	V_{CS} = 0V
Matching characteristics						
Base-emitter voltage difference						
TR1–TR2	$V_{BE1}-V_{BE2}$		2.0	5.0	mV	
TR3–TR4	$V_{BE3}-V_{BE4}$		2.0	5.0	mV	V_{CE} (all transistors) = 5.0V
Large signal current ratio matching						
TR1/TR2	h_{FE1}/h_{FE2}	0.9				I_E (all transistors) = 100μA
TR3/TR4	h_{FE3}/h_{FE4}	0.9				

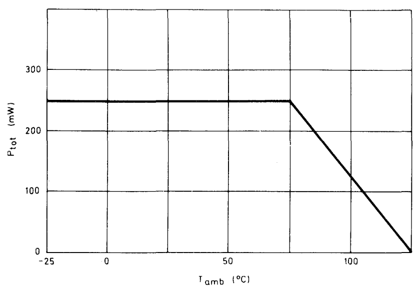


Fig. 2 Power dissipation

ELECTRICAL CHARACTERISTICS – SL355

Test conditions (unless otherwise stated):

T_{amb} = +25°C

Characteristics apply to each transistor

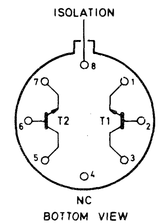
Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Each transistor						
Collector-base breakdown voltage	BV_{CBO}	25			V	I_C = 10μA, I_E = 0
Collector-emitter sustaining voltage	LV_{CEO}	12	18		V	I_C = 5mA, I_B = 0
Emitter-base breakdown voltage	BV_{EBO}	5			V	I_E = 10μA, I_C = 0
Collector-isolation breakdown voltage	BV_{CIO}	25			V	I_C = 10μA
Collector-base leakage current	I_{CBO}		0.3	1	nA	V_{CB} = 10V, I_E = 0
Emitter-base leakage current	I_{EBO}		1	10	nA	V_{EB} = 2V, I_C = 0
Collector-isolation leakage current	I_{CIO}		1	10	nA	V_{CI} = 10V
Large signal current transfer ratio	h_{FE}	10	55			I_C = 100μA, V_{CE} = 5.0V
Transition frequency	f_T		600		MHz	I_C = 5mA, V_{CE} = 5.0V
Collector-isolation capacitance	C_{CI}			6.5	pF	V_{CS} = 0V
Matching characteristics						
Base-emitter voltage difference						
TR1–TR2	$V_{BE1}-V_{BE2}$		2.0	5.0	mV	V_{CE} (all transistors) = 5.0V
TR3–TR4	$V_{BE3}-V_{BE4}$		2.0	5.0	mV	
Large signal current ratio matching						I_E (all transistors) = 100μA
TR1/TR2	h_{FE1}/h_{FE2}	0.9				
TR3/TR4	h_{FE3}/h_{FE4}	0.9				

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL360C
2·5GHz MATCHED TRANSISTOR PAIR

CM8



The SL360C is a bipolar monolithic chip comprising a pair of integrated circuit transistors designed for applications where close parameter matching and thermal tracking are of prime importance. They have a very high f_t (typically 2.5 GHz) and low capacitances.

ELECTRICAL CHARACTERISTICS @ T_{amb} = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	15	32		V	I_C = 10μA
BV_{CEO}	8	15		V	I_C = 10μA
LV_{CEO}	8	14		V	I_C = 5mA
BV_{CIO}	30	60		V	I_C = 10μA
BV_{EBO}	4.8			V	I_E = 10μA
h_{FE}	30	65			V_{CE} = 2V, I_E = 5mA
f_T	1.6	2.5		GHz	V_{CE} = 2.5V, I_E = 5mA, f = 200MHz
		3.2		GHz	V_{CE} = 5V, I_E = 25mA
$V_{BE1} - V_{BE2}$ (note 1)		3	10	mV	V_{CE} = 2V, I_E = 1mA
h_{FE1}/h_{FE2} (note 1)		1.1			V_{CE} = 2V, I_E = 5mA
V_{CE} (Sat)		0.25	0.4	V	I_E = 10mA, I_b = 1mA
C_{ob} (note 2)		0.7		pF	V_{CB} = 0V
C_{TE} (note 2)		1.5		pF	V_{BE} = 0V
C_{CI} (note 3)		2.7		pF	V_{CI} = 0V
V_{be} (on)		720		mV	I_E = 1mA, V_{CE} = 2V
I_{CBO}			1	nA	V_{CB} = 10V
I_{CIO}			1	nA	V_{CE} = 10V
I_{EBO}			1	nA	V_{EB} = 2V

NOTES

1. It is assumed here that device suffixed 1 has the greater numerical value.
2. These capacitances include stray header capacitance which is about 0.1pF.
3. These capacitances include stray header capacitance which is about 0.9pF.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Storage temperature	-55°C to $+175^\circ$C
Operating junction temperature	$+175^\circ$C max.

Maximum Dissipation (Note 5)

Dissipation at 25°C free air temperature	600mW
Dissipation at 100°C free air temperature	300mW

Maximum Voltages

BV_{CBO} : 15V
BV_{CEO} : 8V
BV_{EBO} : 4.8V
BV_{CIO} : 30V (note 6)

4 The maximum ratings are limiting absolute values above which life or satisfactory performance may be impaired.

5. These ratings give a junction temperature of 175° with a junction-to-ambient thermal resistance of 250°C/W (derating factor 4 mW/°C.)

6. The isolation pin should be negative with respect to the collectors.

PLESSEY
SEMICONDUCTORS

SL300 SERIES

MATCHED TRANSISTORS

SL 362C LOW NOISE TRANSISTOR PAIR

CM8

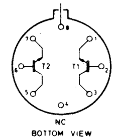


Fig. 1 Pin connections

The SL362C is a bipolar monolithic integrated circuit comprising a pair of transistors designed for applications where low noise and very high frequency operation are of prime importance. A typical noise figure at 60MHz is less than 1.6dB.

ELECTRICAL CHARACTERISTICS @ T_{amb} = 25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	12	24		V	I_E = 10μA
BV_{CEO}	8	15		V	I_C = 10μA
BV_{CIO}	20	40		V	I_C = 10μA
BV_{EBO}	5			V	I_C = 10μA
h_{FE}	30	70			I_E = 1mA, V_{CE} = 2V
		60			I_E = 10mA, V_{CE} = 2V
f_T	1	1.6		GHz	I_E = 2mA, V_{CE} = 2V
	1.4	2.2		GHz	I_E = 10mA, V_{CE} = 10V
$V_{BE1} - V_{BE2}$		5		mV	I_E = 1mA, V_{CE} = 2V
Noise figure (note 1)		1.6	2.0	dB	I_E = 1mA, R_s = 200Ω f = 60MHz
C_{OB}		1.0		pF	V = 0
C_{CI}		0.9		pF	V = 0
C_{TE}		15.0		pF	V = 0

Note 1; The noise figures are quoted at 60MHz. Typically, they are constant from 10kHz to 200MHz.

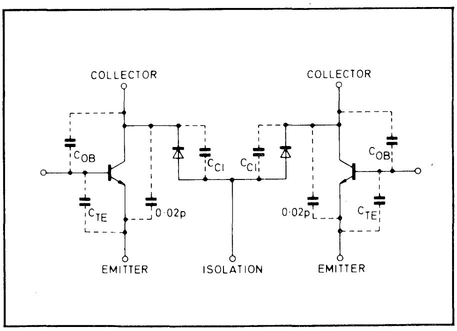


Fig.2 Equivalent circuit

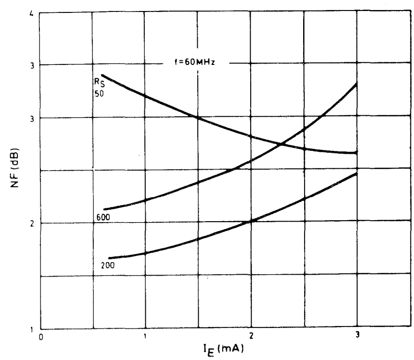


Fig.3 Typical noise figure v. emitter current

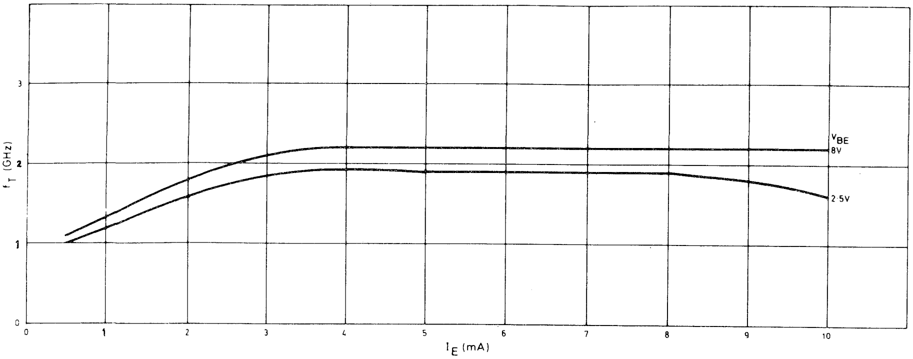


Fig.4 Typical f_T v. emitter current

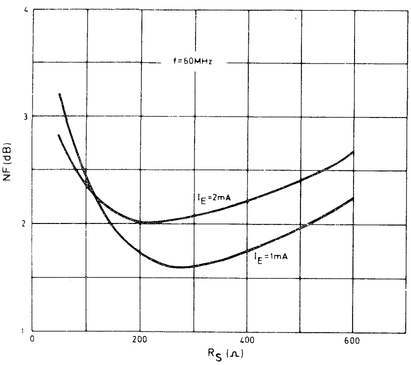


Fig. 5 Typical noise figure v. source impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature		−55°C to +150°C
Operating Junction temperature		150°C
Total Dissipation		300mW
Collector current		50mA
BV_{CBO}	: 12V	
BV_{CEO}	: 8V	
BV_{EBO}	: 5V	
BV_{CIO}	: 20V	

Note: The isolation pin should be negative with respect to the collectors.

SIMPLE FEEDBACK AMPLIFIER (FIG.6)

The amplifier has a response down to DC achieved by the use of a long-tailed pair in the input stage, which also gives low offset voltages and a convenient method of applying negative feedback. The input is applied to Tr 1 and negative feedback applied to Tr 2 via resistors R 6 and R 7. Tr 3 is current-driven from the long-tailed pair and gives the output voltage across R 3. It is important to keep the stray capacitance from R 3 to ground as small as possible for the best high frequency performance. By the use of the very high f_T transistor pair SL360C for Tr 3 and Tr 4 any shunting effect of transistor capacitances across R 3 is reduced.

The frequency response of the amplifier shown in Fig.7 is flat to within ± 1 dB from DC to 240 MHz. The small peak at 200 MHz is not layout dependent but is due to parasitic lead inductance in the transistor packages. Measurements were made with a 50Ω source impedance and a load of 0.1 MΩ + 2.5 pF. The amplifier will drive a 50Ω load up to 150 MHz if required. For simplicity the noise figure was measured with a 50Ω source impedance and a spot noise figure of 4.2 dB was measured at frequencies of 30 to 200 MHz. The calculated variation of noise figure with source impedance is shown in Fig.8, which indicates an optimum noise figure of 2.5 dB at 200Ω source impedance.

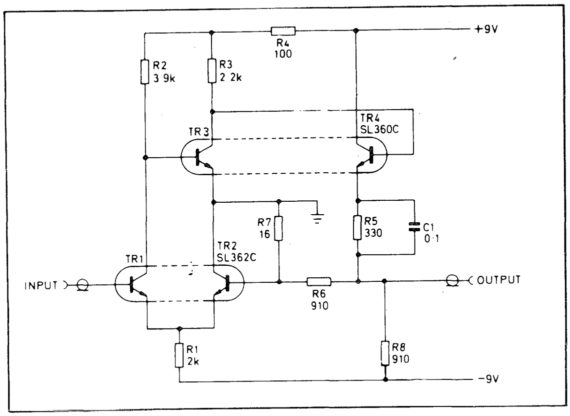


Fig. 6 Circuit diagram

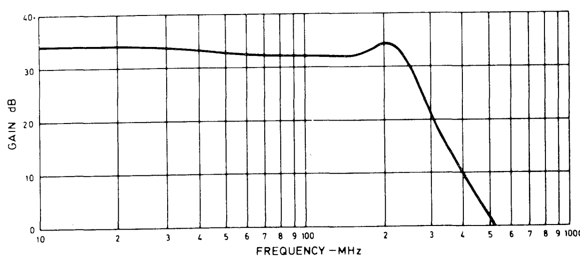


Fig. 7 Frequency response of wide band amplifier

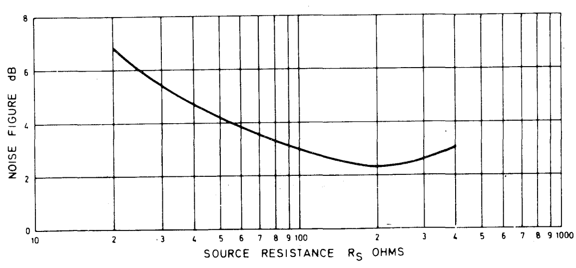


Fig. 8 Calculated noise figure v. source impedance

LAYOUT

It has been found that the circuit is not particularly sensitive to layout change, but the obvious precautions in constructing VHF circuits should be observed. Transistor leads should be kept as short as possible, in particular the emitters of Tr 1, Tr 2 and Tr 3. The leads of R 7 should also be short and if accurate gain stability is not required, a carboncomposition resistor will give minimum inductance.

NOISE REDUCTION

Two techniques are available to reduce the noise figure at low source impedances. One is to use a transformer to produce a source resistance nearer to the optimum of 200Ω. The other method is to connect two transistors in parallel as shown in Figure 9. The effect of this combination is compared with a single transistor in Figure 10. The graph shows the calculated noise figure versus emitter current with a 50Ω source impedance for both long tailed pair and common emitter configurations. As can be seen, a noise figure of 1.6 dB at 50Ω source can be achieved with the arrangement of Figure 9 in a grounded emitter configuration. The parallel connected combination will, of course, have double the output capacitance of the single device, but the effect of this on the high frequency performance can be reduced by feeding into a low impedance. Also, the combination will have a lower f_T than a single transistor at a given operating current. However, if the current is doubled in the combination, little degradation will occur.

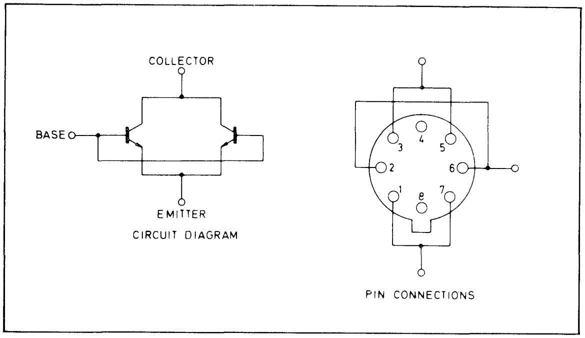


Fig. 9 ***Parallel connection of two transistors***

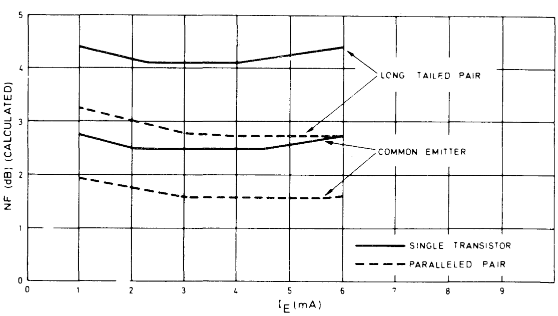


Fig. 10 ***Noise figure at 50Ω source impedance***

PLESSEY
SEMICONDUCTORS

SL500 SERIES
WIDEBAND AMPLIFIERS

SL501A&B SL502A&B SL503A&B
SL551A&B SL552A&B SL553A&B

The SL500 series are bipolar integrated circuit wideband RF amplifiers, developed for use in linear radar IF strips operating at centre frequencies between 10 and 60 MHz. AGC facilities and supply line decoupling are incorporated in the circuits. The mid-band current gain is typically 26dB.

The SL501A and SL501B differ only in current gain and cut-off frequency tolerances. Both are supplied without an output load resistor (free collector). Flatpack versions are SL551A and SL551B, respectively. The SL502A and SL502B are similar to the SL501A and SL501B but incorporate a 1kΩ output load resistor. Flatpack versions are SL552A and SL552B, respectively.

The SL503A and SL503B are similar to the SL501A and SL501B except that the output current swing is typically 5mA. Flatpack versions of SL503A and SL503B are SL553A and SL553B, respectively.

FEATURES

- Upper Cut-off Frequency 100 MHz Typ.
- Mid-Band Current Gain 26 dB Typ.
- AGC Input
- On-chip Supply Decoupling

APPLICATIONS

- Radar IF Strips
- Wideband RF Amplifiers

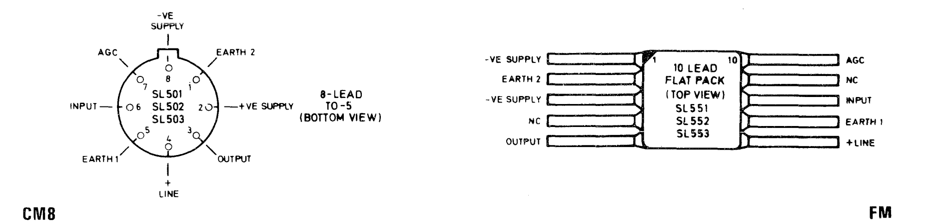
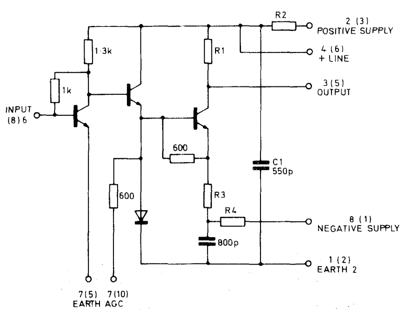


Fig. 1 Pin Connections



	R1	R2	R3	R4
SL501 A & B SL551 A & B	O/C	375Ω	30Ω	1.6kΩ
SL502 A & B SL552 A & B	1kΩ	375Ω	30Ω	1.6kΩ
SL503 A & B SL553 A & B	O/C	250Ω	37Ω	800Ω

PIN NUMBERS FOR THE VARIOUS ENCAPSULATIONS ARE INDICATED THUS:
3 TO-5
(5) FLATPACK

Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions:

Tamb +22°C ± 2°C
Positive supply +6V
Negative supply −6V
AGC not applied unless specified.
R_L = 1kΩ (SL501 and SL551); 390Ω (SL503 and SL553)

Characteristic	Circuit	Value			Units	Test conditions
		Min.	Typ.	Max.		
Current gain	SL501A, SL551A, SL502A, SL552A, SL503A, SL553A.	24	26	28	dB	f = 30MHz
	SL501B, SL551B, SL502B, SL552B, SL503B, SL553B.	23	26	29	dB	f = 30MHz
Upper cut-off frequency (see Fig. 3)	SL501A, SL551A, SL502A, SL552A, SL503A, SL553A.	80	100	120	MHz	680Ω source; 50Ω load.
	SL501B, SL551B, SL502B, SL552B, SL503B, SL553B.	60			MHz	680Ω source; 50Ω load.
Lower cut-off frequency (see Fig. 3)	All types	3	5	7	MHz	680Ω source; 50Ω load
Output swing (before clipping)	SL501A, SL551A, SL501B, SL551B, SL502A, SL552A, SL502B, SL552B.	±1.4	±2.0	±2.8	mA	
	SL503A, SL553A, SL503B, SL553B.	±4.0	±5.0	±6.5	mA	
Noise figure (see Fig. 4)	All types		6		dB	f = 60MHz; 250Ω resistive source.
AGC range (see Fig. 5)	All types		40		dB	680Ω source 50Ω load f = 60MHz AGC signal = +2V
Positive supply current	SL501A, SL551A, SL501B, SL551B, SL502A, SL552A, SL502B, SL552B.	4.1	5.5	7.0	mA	
	SL503A, SL553A, SL503B, SL553B.	6.8	8.6	11.0	mA	
Negative supply current	SL501A, SL551A, SL501B, SL551B, SL502A, SL552A, SL502B, SL552B.	2.2	3.0	3.8	mA	
	SL503A, SL553A, SL503B, SL553B.	5.0	6.3	8.0	mA	

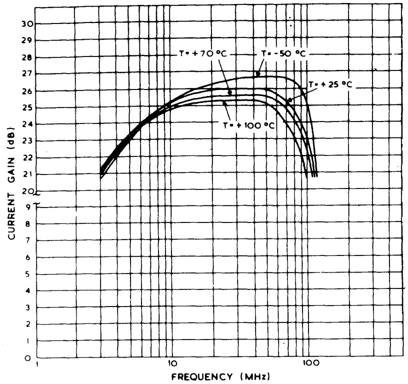


Fig. 3 Frequency response v. temperature

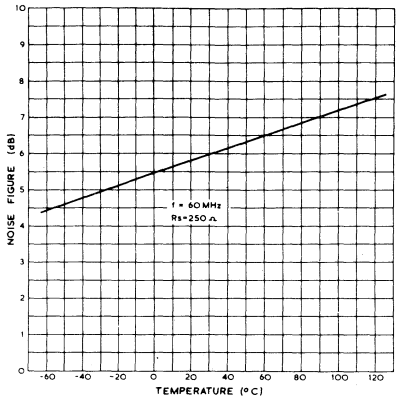


Fig. 4 Noise figure v. temperature

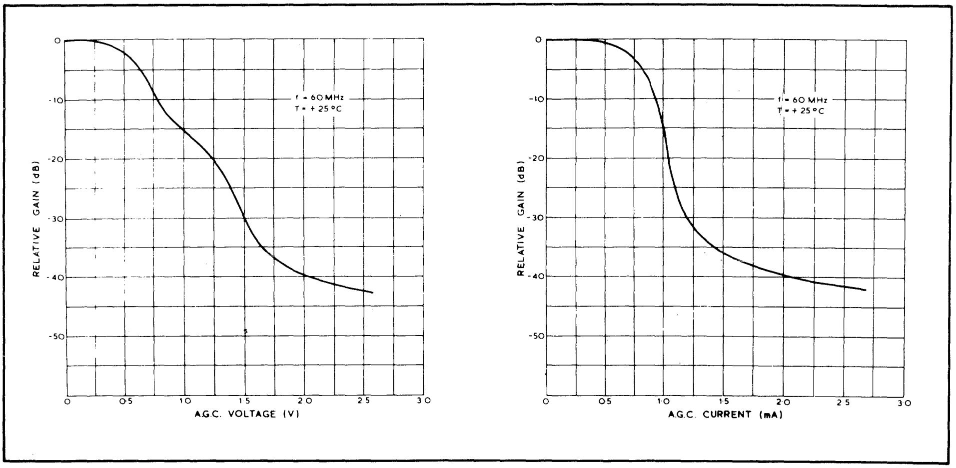
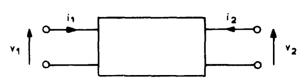


Fig. 5 A.G.C. characteristics

Characteristics of the SL500 series amplifiers expressed in Y parameters are given in Fig. 6 to 9; The parameters are defined as follows:



$$i_1 = Y_{11}v_1 + Y_{12}v_2$$

$$i_2 = Y_{21}v_1 + Y_{22}v_2$$

Where $Y_{11} = G_{11} + jB_{11}$

$Y_{21} = |Y_{21}|e^{j\phi_{21}}$

and $Y_{22} = G_{22} + jB_{22}$

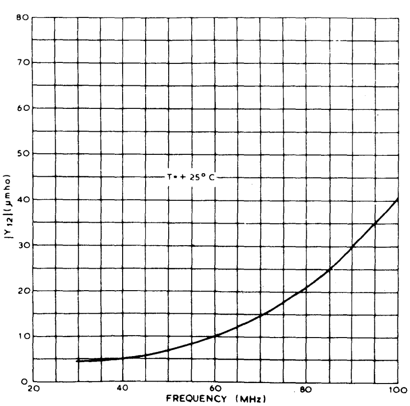
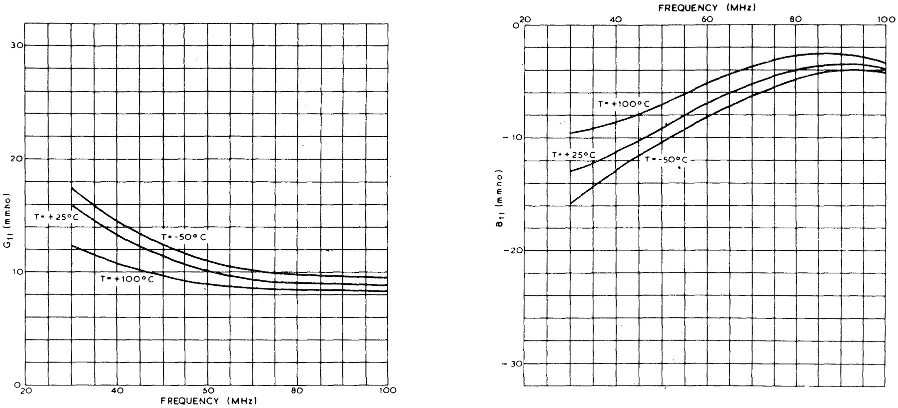
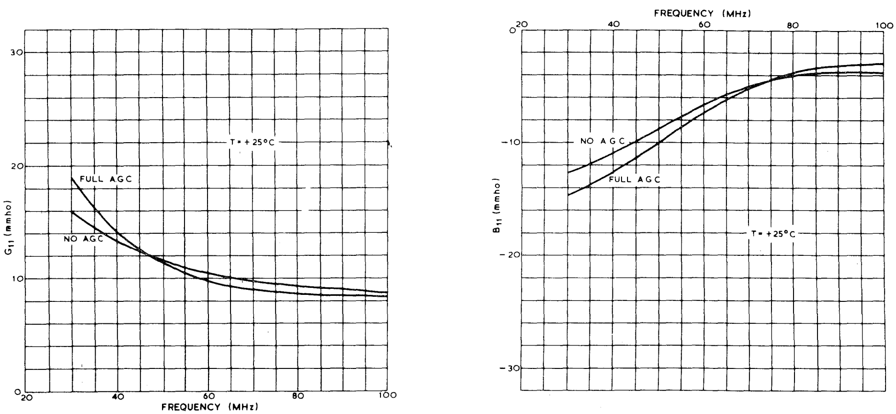


Fig. 7 Feedback admittance (Y_{12})



Typical input admittance v. frequency and temperature (without A.G.C.)



Typical input admittance v. frequency, with and without A.G.C.

Fig. 6 Input admittance (Y_{11})

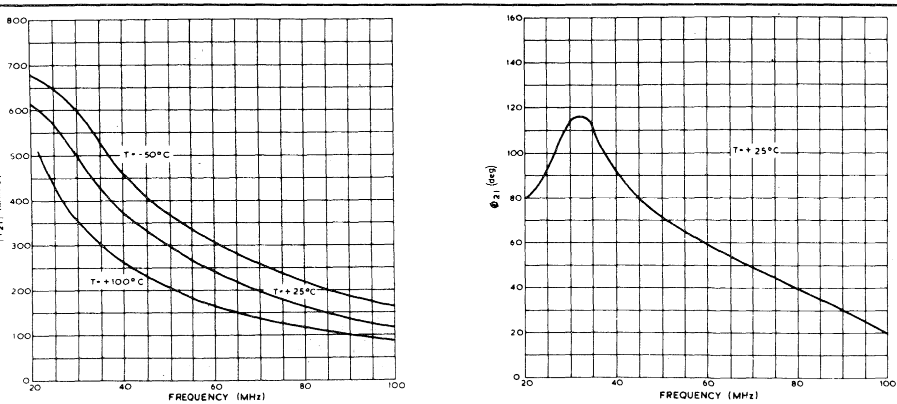
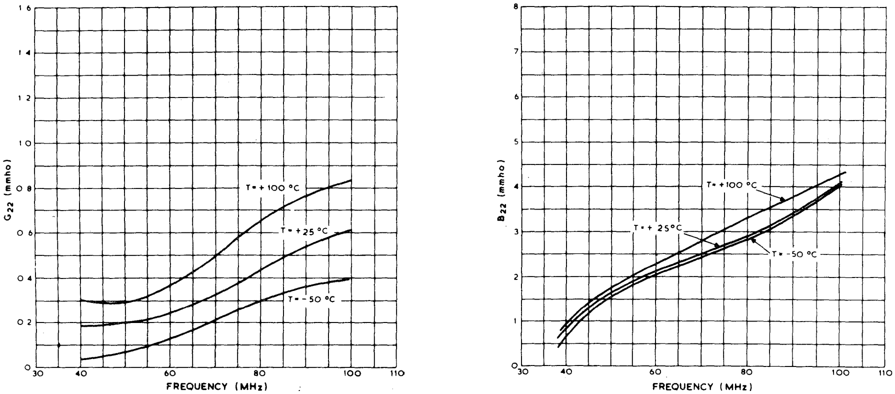
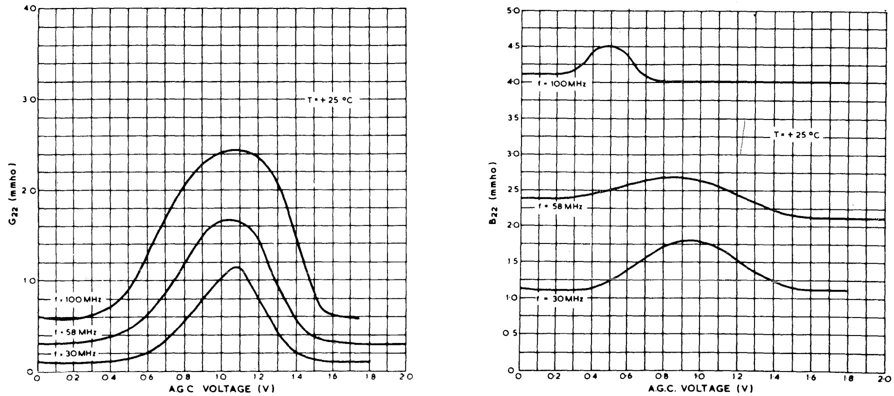


Fig. 8 Forward transfer admittance (Y_{21})



Typical output admittance v. frequency and temperature



Typical output admittance v. A.G.C. voltage

Fig. 9 Output admittance (Y_{22}). These curves apply to SL501A and B, SL503A and B, SL551A and B and SL553A and B. To obtain Y_{22} for SL502A and B and SL552A and B, increase output conductance (G_{22}) by 1mmho and output capacitance by 1pF.

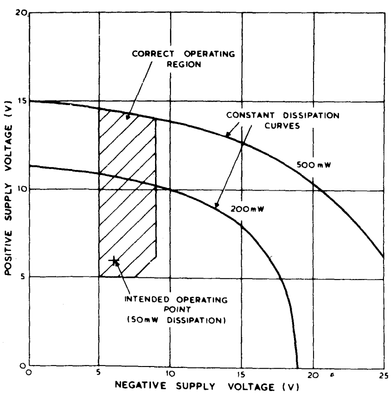


Fig. 10 Absolute maximum supply voltages.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55° to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistanc	80°C/W
Maximum AGC signal	+3.5V or 20mA
Maximum instantaneous voltage (pin 4)	+12V

OPERATING NOTES

The amplifiers are provided with two earth connections to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

The positive supply decoupling capacitor C1 has a series resistance of, typically, 10 ohms. The capacitor is a junction type having a low breakdown voltage and consequently the positive supply current increases rapidly as the supply voltage exceeds 7.5V.

AGC should not be applied to stages required to give output swings in excess of ±0.2mA unless substantial distortion can be tolerated.

SL501 and SL503 devices must be provided with a DC path between pins 3 and 4 for the collector current of the output stage. The DC resistance of this path should not exceed 1000 ohms for the SL501 and 400 ohms for the SL503. The AC load may be connected between pins 3 and 4, or pins 3 and 1. Similar conditions apply to the flatpack versions of these devices, SL551 and SL553, respectively.

PLESSEY
SEMICONDUCTORS

SL510 SERIES
RF DETECTOR/VIDEO AMPLIFIER

SL510C
INCREMENTAL GAIN 11 dB, DC-24MHz
SL511C
INCREMENTAL GAIN 16 dB, DC-14MHz

The SL510C is a bipolar integrated circuit combining the functions of r.f. detection and video amplification. The device is sectionalised to enable the r.f. detector to be used with or without the accompanying video amplifier.

The detector will accept carrier wave signals over a bandwidth from d.c. to 100 MHz. The incremental gain is typically 11dB with a video bandwidth of d.c. to 24 MHz. The circuit will handle pulse widths down to 16ns and the dynamic range is 31dB.

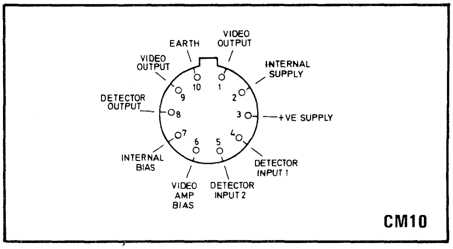


Fig. 1 Pin connections

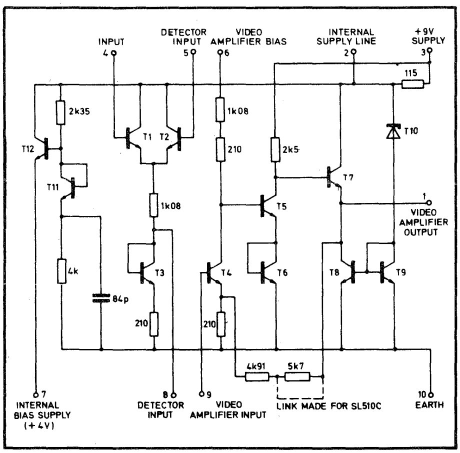


Fig. 2 Circuit diagram

The primary area of application is in the radar field for r.f. pulse detection, and video outputs of 6 volts and 0.5 volts can be driven into 600Ω and 50Ω loads respectively. However, the wide dynamic range of the SL510C also makes it suitable for detection of sine wave amplitude modulation.

The SL511C is of similar design, but has an incremental gain of typically 16dB over a bandwidth of d.c. to 14 MHz. The dynamic range is maintained at 28dB.

The circuits have been allocated the following NATO Stock Numbers:

Type	NATO Stock No.
SL510C	5962-99-038-0470
SL511C	5962-99-038-0471

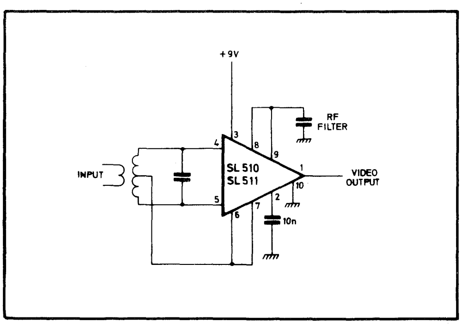


Fig. 3 Full-wave rectification

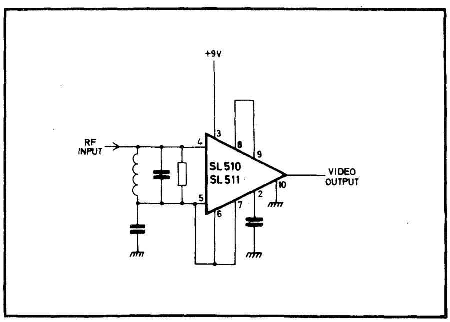


Fig. 4 Half-wave rectification

Electrical Characteristics

Test conditions (unless otherwise stated):

Temperature = +22°C ±2°C
Supply voltage = +9V
External connections: Pin 2 decoupled via 10nF capacitor to earth.
Pin 6 connected to pin 7.
Pin 8 connected to pin 9.

Characteristic	Type	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
Overall incremental gain (1)						
Half-wave	SL510C	3.5	5.5	7.5	dB	See Fig. 3 Detected r.f. is smoothed; centre frequency = 60 MHz
	SL511C	8.0	10.0	12.0	dB	
Full-wave	SL510C		11.5		dB	See Fig. 4
	SL511C		16.0		dB	
Pulse response	Both					
Rise time			16.0	35.0	ns	Output pulse height with respect to 0V = +5V.
Fall time			16.0	35.0	ns	Measurements are from 10% to 90% points on wave form
Positive limiting level at video outputs	Both	5.0	6.0		V	Load impedance = 600Ω; r.f. input at 60 MHz
Quiescent d.c. output voltage	SL510C		0.5	1.0	V	
	SL511C		0.6	1.0	V	
Upper cut-off frequencies						
Detector circuitry	Both		100		MHz	R_s = 25Ω, Z_L = Video input. Vin = 150mV r.m.s., 30% modulated. Output is −1dB with respect to an output at 10 MHz.
Video circuitry	SL510C		24		MHz	Output −3dB R_s = 25Ω Z_L = 600Ω in parallel with 10pF. Measured with respect to an output at 2 MHz.
			35		MHz	Output −6dB
	SL511C		14		MHz	Output −3dB
			21		MHz	Output −6dB
Overall dynamic range (2)						
Half-wave	SL510C		25		dB	See Fig. 3
	SL511C		22		dB	
Full-wave	SL510C		31		dB	See Fig. 4
	SL511C		28		dB	
Current consumption	Both		20	30	mA	
Input impedance to detector (3)	Both					Measured between pins 4 and 5 input level = 600mV r.m.s.; centre frequency = 60 MHz.
Real part		10			KΩ	
Imaginary part			3		pF	
Output impedance from video amplifier	SL510C		6		Ω	Measured at 2 MHz.
	SL511C		12		Ω	
Video amplifier small signal gain	SL510C		27		dB	Measured at 2 MHz. See Fig. 5
	SL511C		33		dB	

NOTES
1. Defined as $\frac{d(\text{video out})}{d(\text{r.f. in})}$
2. Defined as a variation of ±5% in the incremental gain.
3. This parameter is not guaranteed

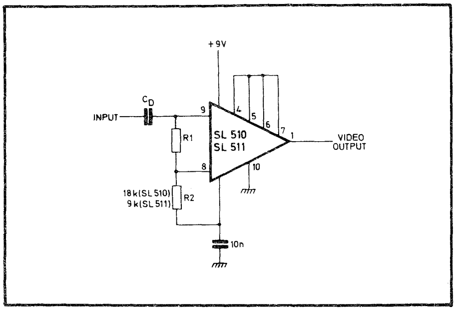


Fig. 5 Video amplification without detection

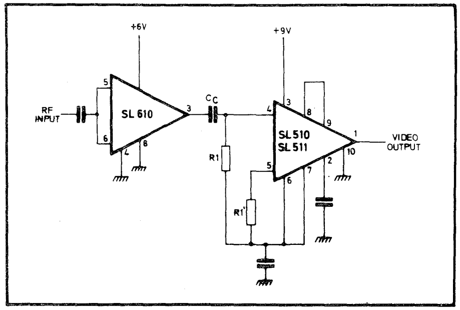


Fig. 7 R-C coupled combination (half-wave), with RF amplification.

OPERATING NOTES

Tuned circuit coupling

There are two basic methods of driving the Detector/Video when used in its normal mode; i.e. from a tuned circuit or via an R-C network. In the former case both full-wave and half-wave rectification are possible using the configurations shown in Figs. 3 & 4 respectively. When the internal bias supply is being used, as illustrated, the quiescent current level of the current source will be drawn from the supply, and the current level in the output stage of the video amplifier will be reduced accordingly. For connection to an external bias supply allowance must be made for 2mA required to drive the video amplifier bias, (pin 6).

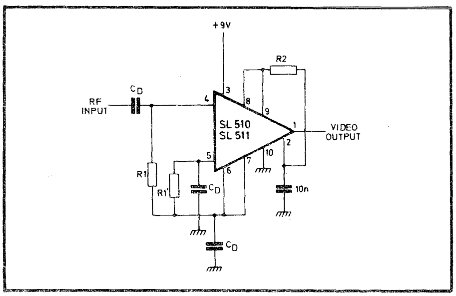


Fig. 6 R-C coupling mode (half-wave)

R-C coupling

R-C input coupling is illustrated in Fig. 6. Decoupling capacitors, C_D, should offer low a.c. impedances relative to the series resistors, R1, at the frequency of the input. Voltage drops arising through input base currents flowing in the series resistors will be amplified and will depress the d.c. quiescent output of the video amplifier. For low β devices this can be excessive and should be offset by introducing resistor R2 which injects current into pin 8 to raise the output level. With R2 connected to the internal supply line, as shown, the d.c. output voltage will be 52/R2 (±25%) for the SL510C and 26/R2 (±25%) for the SL511C where R2 is in kΩ.

Fig. 5 illustrates this technique applied to the use of the circuit for video amplification without detection, where it may be necessary to set the output quiescent voltage midway between the internal supply line and earth. Input coupling is via C_D/R2, where the reactance of C_D is chosen to be low compared with R2. Since the video amplifier response extends down to d.c. R2 must be small to limit the input voltage error due to the base current flowing in R2. This can be overcome by using an r.f. choke with low d.c. resistance.

SL610/11/12 – SL510/11 Combination

The simplest method of connection is shown in Fig. 7 using R-C coupling. In view of the bandwidths involved due care in layout must be observed (note that the output earth of the SL510 is taken forward to the video-detector earth). For tuned coupling refer to the SL610/11/12 data sheet.

Absolute Maximum Ratings

Storage Temperature	–55°C to +175°C
Operating Temperature	–55°C to +125°C
Supply Voltage	+12 Volts

CIRCUIT DESCRIPTION

The circuit (Fig. 2) incorporates a long tailed pair detector, with both input bases (pins 4 and 5) accessible so that it can be driven either full-wave or half-wave, as illustrated in the application notes. The output (pin 8) is taken from an attenuation chain at a level suitable to drive the video amplifier (input pin 9). With r.f. filtering between pins 8 and 9 (the usual mode of operation) the input level to the video amplifier will reduce to the mean value of the detected r.f. i.e. ($2/\pi$ x peak output) for full-wave rectification and ($1/\pi$ x peak output) for half-wave rectification.

The video amplifier is directly coupled throughout and essentially consists of two stages of gain TR4 and TR5, and an emitter follower output stage TR7 with overall feedback to the emitter of TR4. Pin 6, the video amplifier bias, should be taken to the same d.c. potential as pins 4 and 5 to ensure that the quiescent output level is tolerant of variations in this potential. In this condition the output is at a 'zero' quiescent level (nominally +600 mV), which allows direct coupling to the load, a convenient feature since output pulses are uni-directional when driving from the detector.

The internal bias supply at pin 7 is an emitter follower biased from the supply line and an external current drain is required to establish its quiescent current.

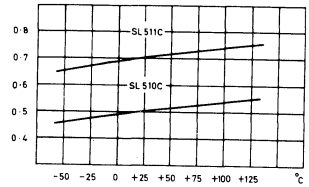


Fig. 8 Change in quiescent d.c. output voltage v. temperature

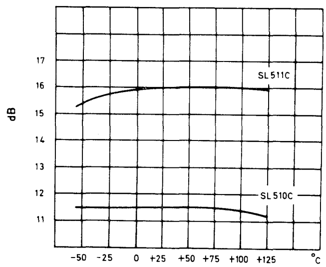


Fig. 10 Change in overall incremental gain v. temperature

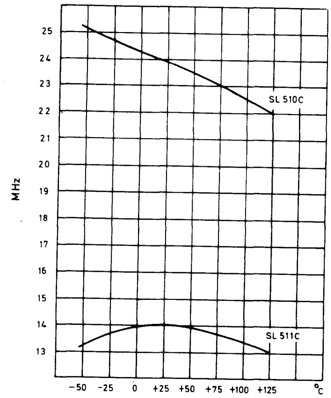


Fig. 9 Change in upper 3dB point for video amplifier v. temperature

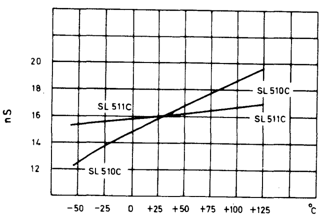


Fig. 11 Change in rise/fall time with temperature

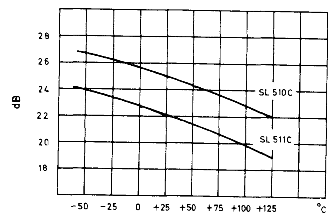


Fig. 12 Change in dynamic range (half-wave) with temperature

PLESSEY
SEMICONDUCTORS

SL521 SERIES
WIDEBAND AMPLIFIERS

SL521A, B & C SL571A, B & C

The SL521A, B and C are bipolar monolithic integrated circuit wideband amplifiers, intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 100MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL521 is typically 12 dB (4 times). The SL521A, B and C differ mainly in the tolerance of voltage gain and upper cut-off frequency. The SL521A, B and C versions have T0-5 encapsulation; the flatpack versions are also available, designated SL571A, B and C.

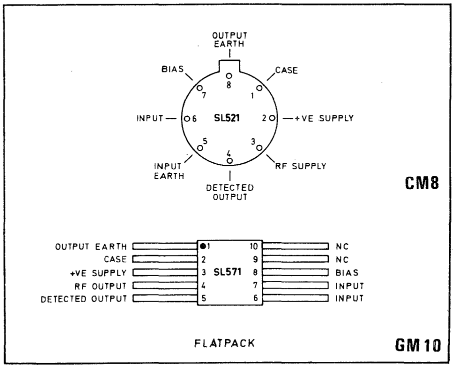


Fig. 1 Pin connections

FEATURES

- Well-defined Gain
- 4dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 165MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF strips with Gains up to 108 dB and Linearity Better Than 1 dB.

ABSOLUTE MAXIMUM RATINGS
(Non-simultaneous)

Storage temperature range	–55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

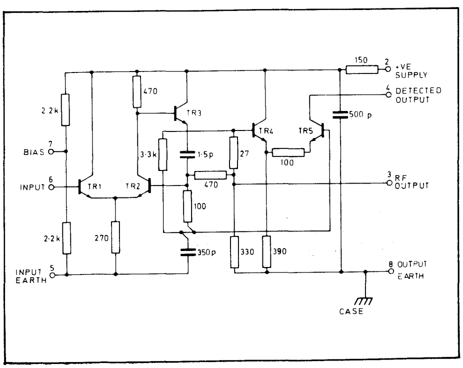


Fig. 2 SL521 Circuit diagram

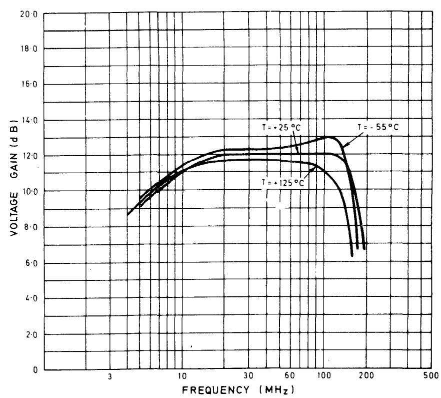


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature = +22°C ± 2°C
Supply voltage = +6V
DC connection between input and bias pins.

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain, f = 30MHz	SL521A, SL571A	11.5		12.5	dB	10 ohms source, 8pF load
	SL521B, SL571B	11.3		12.7	dB	
	SL521C, SL571C	11.0		13.0	dB	
Voltage gain, f = 60MHz	SL521A, SL571A	11.3		12.7	dB	
	SL521B, SL571B	11.0		13.0	dB	
	SL521C, SL571C	10.7		13.3	dB	
Upper cut-off frequency (Fig. 3)	SL521A, SL571A	150	170		MHz	10 ohms source, 8pF load
	SL521B, SL571B	140	170		MHz	
	SL521C, SL571C	130	170		MHz	
Lower cut-off frequency (Fig. 3)	All types		5	7	MHz	10 ohms source, 8pF load
Propagation delay	All types		2		ns	
Maximum rectified video output current (Fig. 4 and 5)	SL521A, SL571A	1.00		1.10	mA	f = 60MHz, 0.5V rms input
	SL521B, SL571B	0.95		1.15	mA	
	SL521C, SL571C	0.90		1.20	mA	
Variation of gain with supply voltage	All types		0.7		db/V	
Variation of maximum rectified output current with supply voltage	All types		25		%/V	
Maximum input signal before overload	All types	1.8	1.9		V rms	See note below
Noise figure (Fig. 6)			4	5.25	dB	f = 60MHz, Rs = 450 ohms
Supply current	SL521A, SL571A	12.5	15.0	18.0	mA	
	SL521B, SL571B					
	SL521C, SL571C	11.5	15.0	19.0	mA	
Maxiumum RF output voltage			1.2		Vp-p	

Note: Overload occurs when the input signal reaches a level sufficient to forward bias TR1 base-collector junction on peaks.

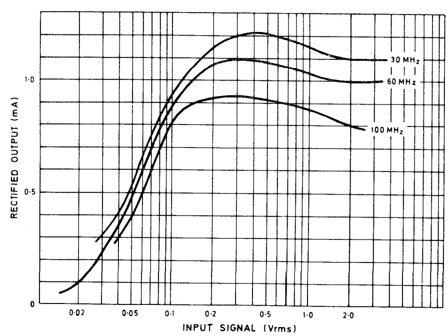


Fig. 4 Rectified output current v. input signal

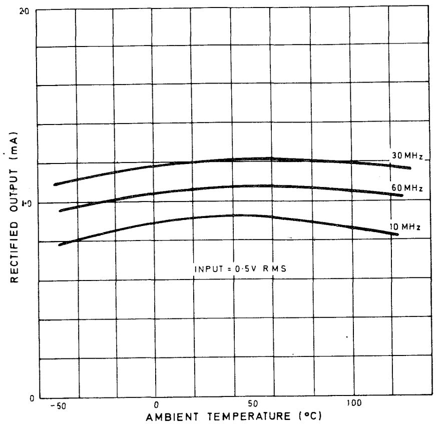


Fig. 5 Maximum rectified output current v. temperature

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8 (This figure shows the TO-5 version.)

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rises times are required. Alternative arrangements may be derived, based on the parasitic parameters given.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

The 500pF supply decoupling capacitor has a resistance of, typically, 10 ohms. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (see ABSOLUTE MAXIMUM RATINGS).

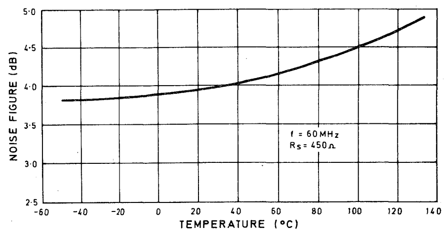


Fig. 6 Typical noise figure v. temperature

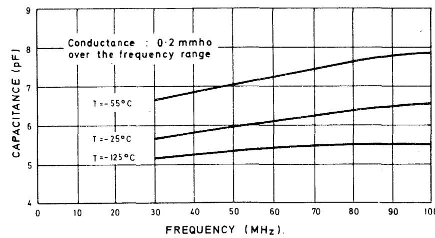


Fig. 7 Input admittance with open-circuit output

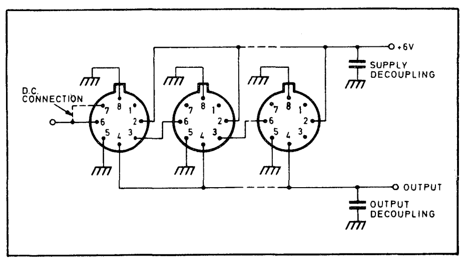


Fig. 8 Direct coupled amplifiers

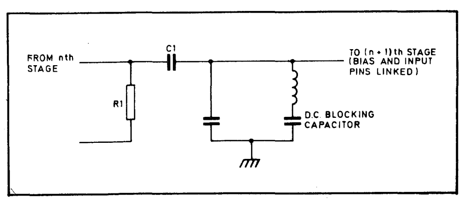


Fig. 9 Suitable interstage tuned circuit

Parasitic Feedback Parameters (Approximate)

The quotation of these parameters does not indicate that elaborate decoupling arrangements are required; the amplifier has been designed specifically to avoid this requirement. The parameters have been given so that the necessity or otherwise of further decoupling, may become a matter of calculation rather than guess-work.

$$\frac{\tilde{I}_4}{V_6} = \frac{\text{RF current component from pin 4}}{\text{Voltage at pin 6}} = 20 \text{ mmhos}$$

(This figure allows for detector being forward biased by noise signals)

$$\frac{V_6}{V_4} = \frac{\text{Effective voltage induced at pin 6}}{\text{Voltage at pin 4}} = 0.003$$

$$\frac{I_2}{V_6} = \frac{\text{Current from pin 2}}{\text{Voltage at pin 6}} = 6\text{mmhos } (f = 10\text{MHz})$$

$$\left[\frac{V_6}{V_2}\right]_a = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.03 \ (f = 10\text{MHz})$$

Voltage at pin 2
(pin 6 joined to pin 7 and
fed from 300 ohms source)

$$\left[\frac{V_6}{V_2}\right]_b = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.01 \ (f = 10\text{MHz})$$

Voltage at pin 2
(pin 7 decoupled)

$\frac{I_2}{V_6}$ $\left[\frac{V_6}{V_2}\right]_a$ $\left[\frac{V_6}{V_2}\right]_b$ decrease with frequency above 10MHz at 6 dB/octave.

Note that the pin numbers above refer to the T0-5 version (SL521A, B and C).

PLESSEY
SEMICONDUCTORS

SL500 SERIES
WIDEBAND AMPLIFIERS

SL525C
WIDEBAND LOG IF STRIP AMPLIFIER

The SL525C is a bipolar monolithic integrated circuit wideband amplifier, intended primarily for use in successive detection logarithmic I.F. strips, operating at centre frequencies between 10MHz and 60MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL525C is typically 12dB.

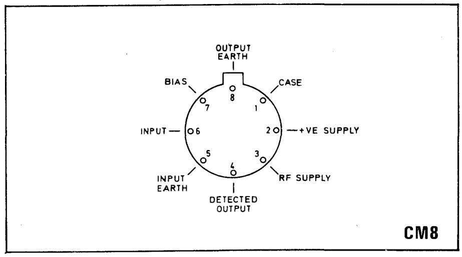


Fig. 1 Pin connections

FEATURES

- Well-defined Gain
- 4dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 150 MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF strips with Gains up to 108 dB and Linearity Better Than 1 dB.

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +175°C
Operating Temperature range	−20°C to +100°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

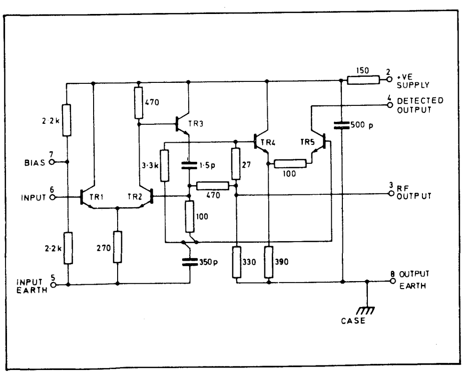


Fig. 2 Circuit diagram

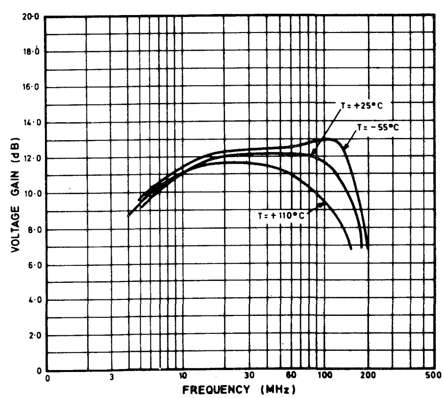


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):—
T_A = +22°C ±2°C
Supply voltage = +6V
DC connection between input and bias pins

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10.5		13.5	dB	f = 30MHz, R_S = 10Ω, C_L = 8pF
	10.0		14.0	dB	f = 60MHz, R_S = 10Ω, C_L = 8pF
Upper cut-off frequency (Fig. 3)	120	150		MHz	R_S = 10Ω, C_L = 8pF
Lower cut-off frequency (Fig. 3)		5	7	MHz	R_S = 10Ω, C_L = 8pF
Propagation delay		2		ns	
Max. rectified video output current (Figs. 4 and 5)	0.85		1.25	mA	f = 60MHz, V_{in} = 500mV rms
Variation of gain with supply voltage		0.7		dB/V	
Variation of maximum rectified output current with supply voltage		25		%/V	
Maximum I/P signal before overload	1.8	1.9		Vrms	See note 1
Noise figure (Fig. 6)		4	5.25	dB	f = 60MHz, R_S = 450Ω
Maximum RF output voltage		1.2		Vp-p	
Supply current		15		mA	

NOTE
1. Overload occurs when the input signal reaches a level sufficient to forward-bias the base-collector junction of TR1 on peak.

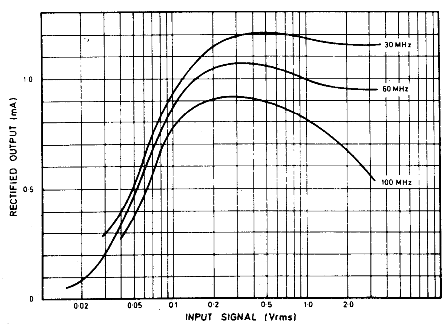


Fig. 4 Rectified output current v. input signal

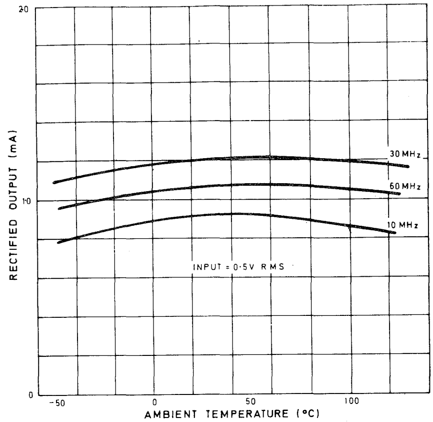


Fig. 5 Maximum rectified output current v. temperature

The 500pF supply decoupling capacitor has a resistance of, typically, 10 ohms. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (see ABSOLUTE MAXIMUM RATINGS).

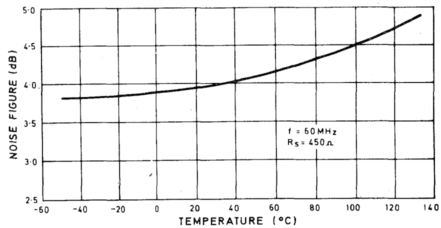


Fig. 6 Typical noise figure v. temperature

OPERATING NOTES

The amplifiers are intended for use directly-coupled, as shown in Fig. 8

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rises times are required. Alternative arrangements may be derived, based on the parasitic parameters given.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

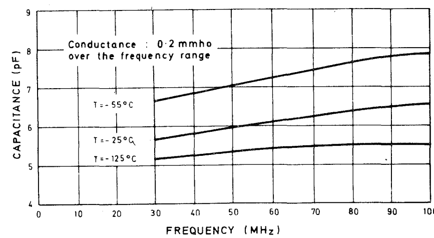


Fig. 7 Input admittance with open-circuit output

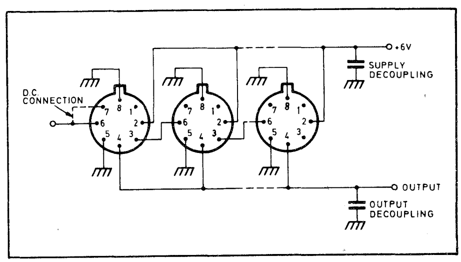


Fig. 8 Direct coupled amplifiers

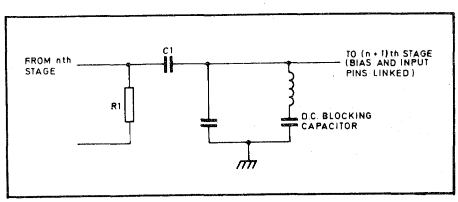


Fig. 9 Suitable interstage tuned circuit

Parasitic Feedback Parameters (Approximate)

The quotation of these parameters does not indicate that elaborate decoupling arrangements are required; the amplifier has been designed specifically to avoid this requirement. The parameters have been given so that the necessity or otherwise of further decoupling, may become a matter of calculation rather than guess-work.

$$\frac{\tilde{I}_4}{V_6} = \frac{\text{RF current component from pin 4}}{\text{Voltage at pin 6}} = 20 \text{ mmhos}$$

(This figure allows for detector being forward biased by noise signals)

$$\frac{V_6}{V_4} = \frac{\text{Effective voltage induced at pin 6}}{\text{Voltage at pin 4}} = 0.003$$

$$\frac{I_2}{V_6} = \frac{\text{Current from pin 2}}{\text{Voltage at pin 6}} = 6\text{mmhos } (f = 10\text{MHz})$$

$$\left[\frac{V_6}{V_2}\right]_a = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.03 \ (f = 10\text{MHz})$$

Voltage at pin 2
(pin 6 joined to pin 7 and
fed from 300 ohms source)

$$\left[\frac{V_6}{V_2}\right]_b = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.01 \ (f = 10\text{MHz})$$

Voltage at pin 2
(pin 7 decoupled)

$\frac{I_2}{V_6}$ $\left[\frac{V_6}{V_2}\right]_a$ $\left[\frac{V_6}{V_2}\right]_b$ decrease with frequency above 10MHz at 6 dB/octave.

PLESSEY
SEMICONDUCTORS

SL530C

TRUE LOG. AMPLIFIER

GENERAL DESCRIPTION

The SL530C is a monolithic non-linear integrated circuit designed to realise a logarithmic transfer function in high-gain amplifier strips at frequencies between 4 and 80 MHz. THE DEVICE IS SO DESIGNED THAT INPUT SIGNAL PHASE INFORMATION IS RETAINED. A typical dynamic range of 70 dB can be achieved over a bandwidth of 10 MHz.

The operation of the SL530C relies upon the principle that amplifiers with an input/output characteristic as shown in Fig. 1 can be cascaded to produce the straight line approximation to a logarithmic law shown in Fig. 2. This may be represented by the expression:

$$V_{out} = K1 \ Log_{K2}\left(1 + \frac{V_{in}}{K3}\right)$$

Where K1, K2, K3 are scaling constants.

The logarithmic law remains true for any value of A or V_L (the breakpoint with respect to input or output) providing cascaded units are similar. It depends only upon the slope gain after limiting: this must be unity. Differences in this slope gain between the devices used in the strip will cause ripples in the log response, whilst the values of A, V_L and n determine the dynamic range available.

Dynamic Range

When Vin $\geqslant V_{LO}$ then all stages of the strip are operating in the unity gain mode. As n (the number of stages in the strip) is increased, the minimum input voltage for the onset of the logarithmic law is V_{LO}/A^n. The input dynamic range is therefore A^n or n20 logA dB. In other words, the dynamic range equals the low level strip gain.

If this level is as low as the effective noise input voltage, the addition of further stages does not result in any increase in dynamic range. For $R_S = 50\Omega$ the effective noise input voltage is approximately $3nV/\sqrt{Hz}$ The maximum dynamic range is thus given by:

$$\text{Dynamic Range} = \frac{V_{LO}}{3 \times 10^{-9}\sqrt{B}} \quad \text{Where B = Bandwidth}$$

$$\approx \frac{15 \times 10^6}{\sqrt{B(Hz)}} \qquad (V_{LO} \approx 45mV)$$

Hence for a bandwidth of 10 MHz, dynamic range = 73 dB, and the number of amplifier stages is six.

Unity Gain Slope

The logarithmic accuracy of a strip is dependent upon the consistent accuracy of this slope from device to device. The frequency response of the IC shows some peaking above 50 MHz but this may be reduced by a resistor in series with the output from pin 6. A typical value is between 0 and 50Ω.

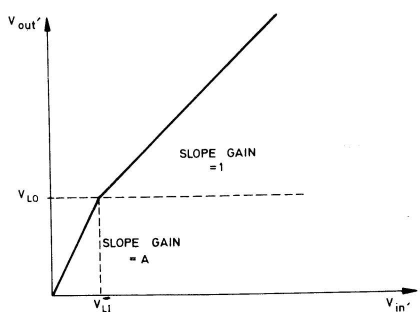


Fig. 1 Device transfer characteristic

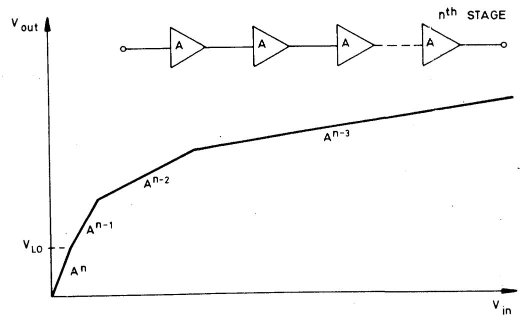


Fig. 2 n-stage strip-transfer characteristic

ELECTRICAL CHARACTERISTICS

Test Conditions: Positive supply 6 volts
Ambient temperature +22°C ± 2°C (unless otherwise stated)
D.C. connection Pin 4 to Pin 5
Output of each device loaded by input of next.

Characteristic	Value Min.	Typ.	Max.	Units	Test Conditions
Midband gain low level	11.6	13.6	15.6	db	V_{in} = 2 mV rms, f = 30 MHz
Slope gain high level	−1	0	+1	dB	V_{in} = 100 mV rms, f = 30MHz
Upper cut-off frequency	60	90		MHz	−3dB w.r.t. f = 30 MHz
Lower cut-off frequency			4	MHz	−3dB w.r.t. f = 30 MHz
Phase change		±5.5	±12	Degrees	f = 30 MHz , V_{in} = 2 – 600mV rms.
Gain change		±0.5		dB	Vin = 100 mV, f = 30 MHz, T_A = −55°C to 125°C
Voltage at Pin 4 and Pin 5		1.75		V	Measured w.r.t. earth
Supply current		20	25	mA	

Note: Pins 3, 7, 8 are intended to enable system currents to be directed to their proper location, thus avoiding earth loops. All these pins must be at the same d.c. potential.

OPERATING NOTES

The layout should be in-line and compact, using physically small components. Provided this is the case an earth plane is not necessary even though the strip is boxed eventually. It may be necessary to use an input isolating transformer of 1:1 turns-ratio in which instance the box should only be connected to the outer screens of the co-axial connectors at input and output and to pin 7 of the output stage.

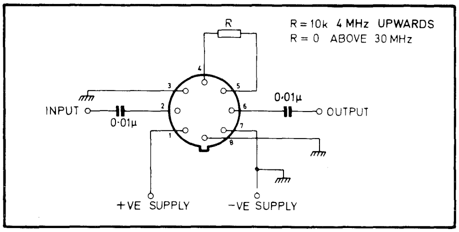


Fig. 3 Typical circuit connection

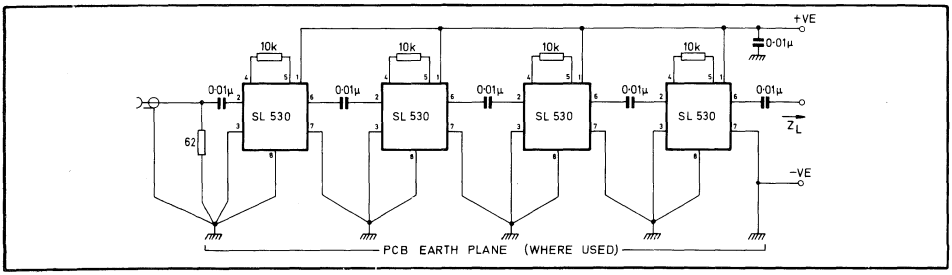


Fig. 4 Typical 4-stage strip

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	−55°C to +125°C
Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Operating voltage Pin 2	3 V

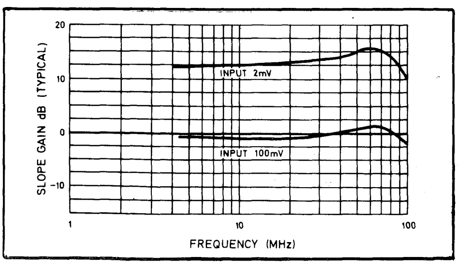


Fig. 5 Frequency response

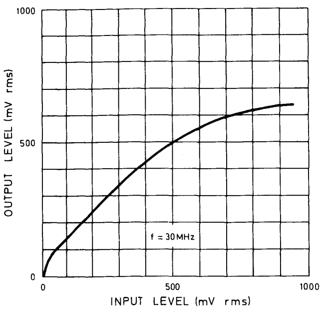


Fig. 6 Transfer characteristic

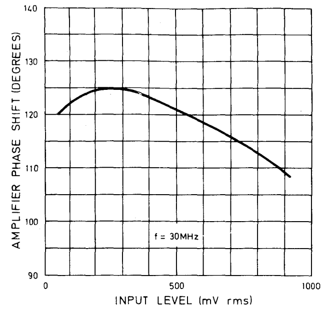


Fig. 7. Phase shift v. input

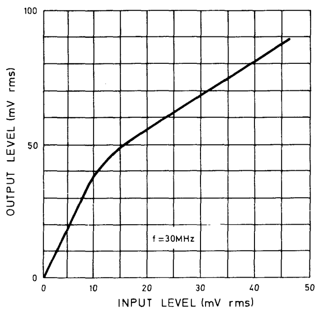


Fig. 8 Transfer characteristic

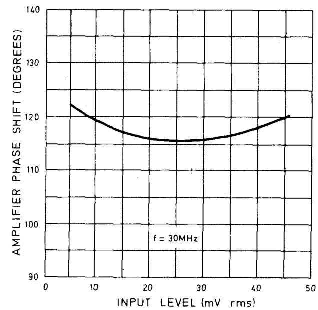


Fig. 9 Phase shift v. input

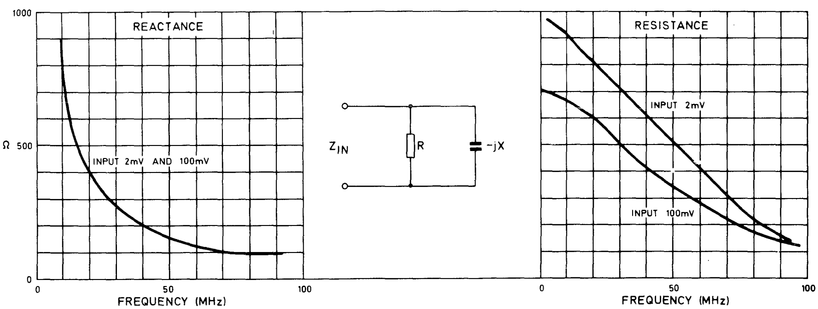


Fig. 10 Input impedance v. frequency

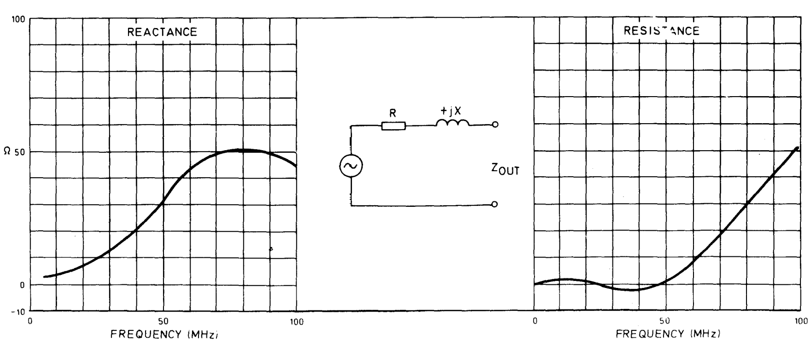


Fig. 11 Output impedance v. frequency

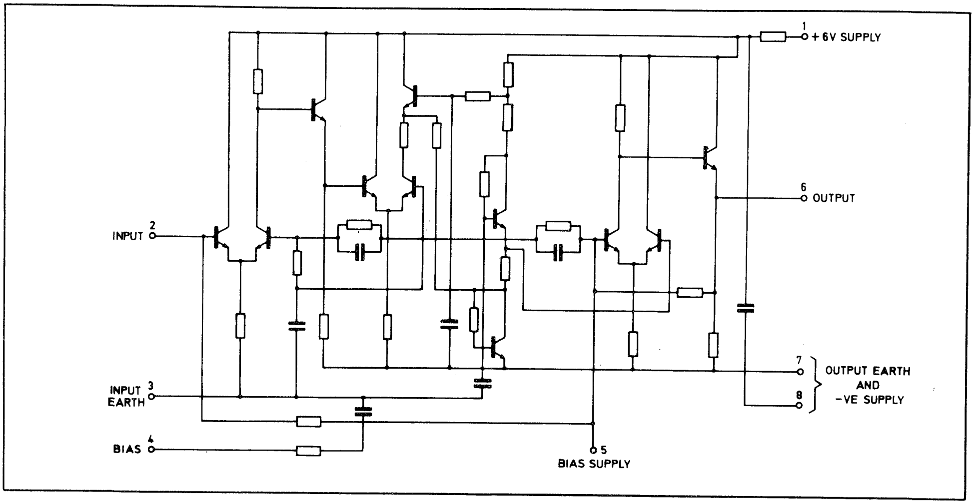


Fig. 12 SL530C circuit diagram
(equivalent only)

PLESSEY SEMICONDUCTORS

SL500 SERIES
WIDEBAND AMPLIFIERS

SL541C
HIGH SPEED VIDEO AMPLIFIER

The SL541C is a monolithic amplifier designed for optimum pulse response and applications requiring high slew rate with fast settling time to high accuracy. The high open loop gain (70dB) is stable with temperature, allowing the desired closed loop gain to be achieved using standard operational amplifier techniques. The device has been designed for optimum response at a gain of 20dB when no compensation is required.

APPLICATIONS

- Wideband IF Amplification
- Wideband Video Amplification
- Fast Settling Pulse Amplifiers
- High Speed Integrators
- D/A and A/D Conversion
- Fast Multiplier Preamps

FEATURES

- High Slew Rate: 175V/μs
- Fast Settling Time: 1% in 50ns
- Open Loop Gain: 70dB
- Wide Bandwidth: DC to 100MHz at 20dB Gain
- Very Low Thermal Drift: 0.02dB/°C Temperature Coefficient of Gain

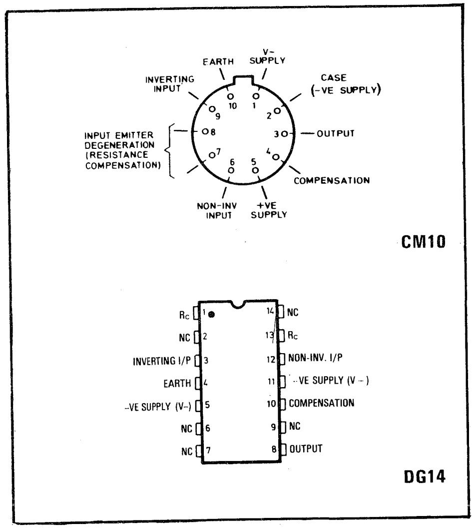


Fig. 1 Pin connections

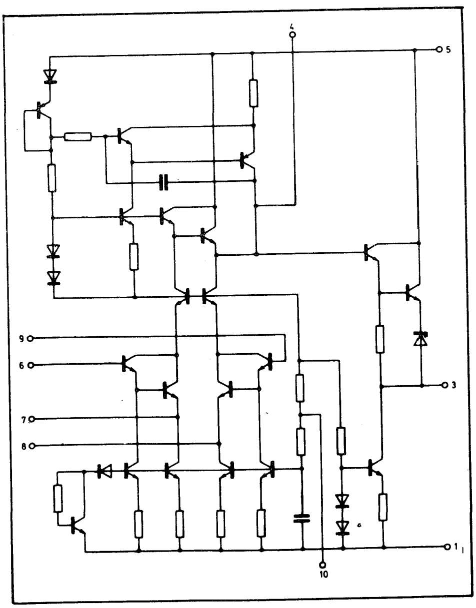
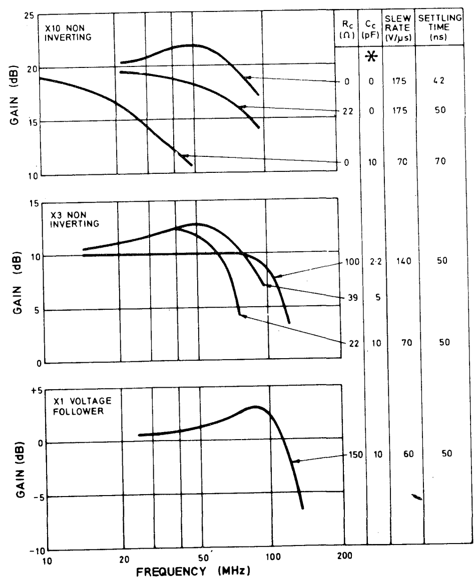


Fig. 2 SL541C circuit diagram (TO – 5 pin nos.)



Rc (Ω)	Cc (pF)	SLEW RATE (V/μs)	SETTLING TIME (ns)
*			
0	0	175	42
22	0	175	50
0	10	70	70
100	2·2	140	50
39	5		
22	10	70	50
150	10	60	50

Fig. 3 Performance graphs – gain v. frequency (load = 2kΩ//10pF)
** See operating note 2*

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Pin 5: +12V
Pin 1: −6V
Pins 7 & 8: Connected together
T_{amb}: 25°C

Characteristic	Value			Units	Test Conditions
	Max.	Typ.	Max.		
Static nominal supply current	–	16	21	mA	
Input bias current	–	7	15	μA	
Dynamic open loop gain	60	71	–	dB	600Ω Load
Open loop temp. co-efficient		−0.02		dB/°C	
Closed loop bandwidth (−3dB)		100		MHz	x 10 gain
Slew rate (4V peak)	100	175		V/μs	x 10 gain
Settling time to 1%		50	100	ns	
Maximum output voltage	±2.5	±3.0		V	
Maximum output current	4	6.5		mA	
Maximum input voltage	±3			V	Non-inverting mode
Supply line rejection (pin 5)	54	66		dB	
(pin 1)	46	54		dB	

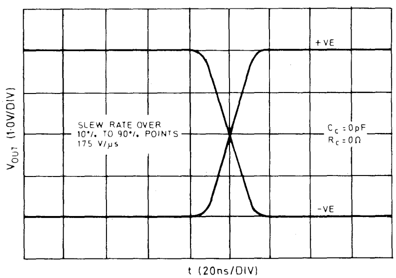


Fig. 4 Slew rate – X10 non-inverting mode

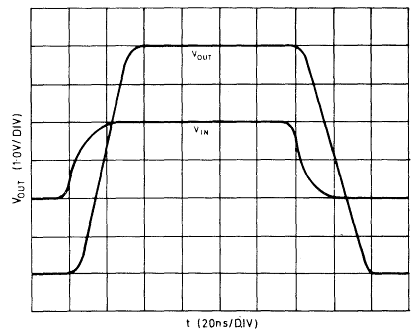


Fig. 6 Output clipping levels – X10 non-inverting mode Input moderately overdriven, so that ouput goes into clipping both sides

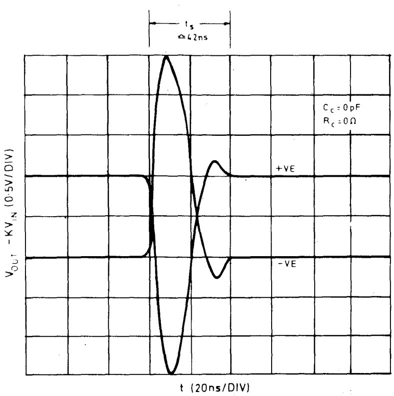


Fig. 5 Settling time – X10 non-inverting mode

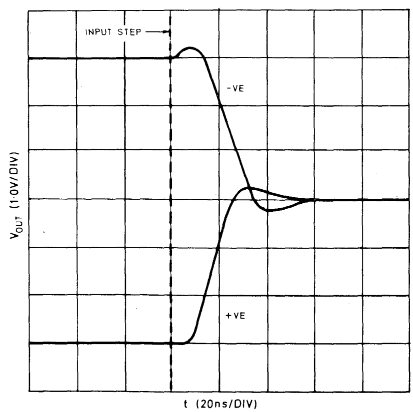


Fig. 7 Output clipping levels – X10 non-inverting mode. Output goes from clipping to zero volts. V_{in} = 3V peak step, offset +ve or −ve.

TEST CONDITIONS AND DEFINITIONS

Both slew rate and settling time are measures of an amplifier's speed of response to an input. Slew rate is an inherent characteristic of the amplifier and is generally less subject to misinterpretation than is settling time, which is often more dependent upon the test circuit than the amplifier's ability to perform.

Slew rate defines the maximum rate of change of output voltage for a large step input change and is related to the full power frequency response (f_p) by the relationship.

$$S = 2\pi f_p E_o$$

where E_o is the peak output voltage

Settling time is defined as the time elapsed from the application of a fast input step to the time when the amplifier output has entered and remained within a specified error band that is symmetrical about the final value. Settling time, therefore, is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of some value of output voltage, plus a period to recover from overload and settle within the given error band.

The SL541 is tested for slew rate in a X10 gain configuration.

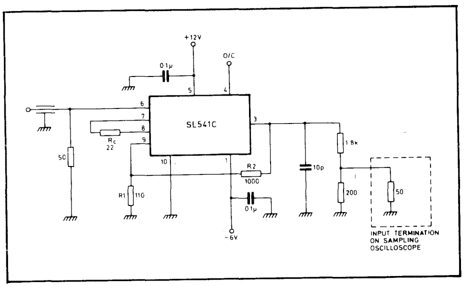


Fig. 8 Non-inverting high speed X10 amplifier test circuit. (TO – 5 pin nos.)

OPERATING NOTES

The SL541 may be used as a normal, but non saturating operational amplifier, in any of the usual configurations (amplifiers, integrators etc.), provided that the following points are observed:

1. Positive supply line decoupling back to the output load earth should always be provided close to the device terminals.
2. Compensation capacitors should be connected between pins 4 and 5. These may have any value greater than that necessary for stability without causing side offsets.
3. The circuit is generally intended to be fed from a fairly low impedance (⩽1kΩ), as seen from pins 6 and 9 – 100Ω or less results in optimum speed.
4. The circuit is designed to withstand a certain degree of capacitive loading (up to 20pF) with virtually no effect. However, very high capacitive loads will cause loss of speed due to the extra compensation required and asymmetric output slew rates.
5. Pin 10 does not need to be connected to zero volts except where the clipping levels need to be defined accurately w.r.t. zero. If disconnected, an extra ±0.5 volt uncertainty in the clipping levels results, but the separation remains. However, the supply line rejection is improved if pin 10 can be left open-circuit.

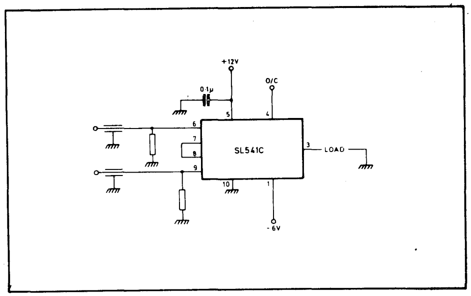


Fig. 9 Non-saturating sense amplifier (30V/μs for 5mV). Note: the output may be caught at a pre-determined level. (TO – 5 pin nos.)

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V^+ to V^-)	24V
Input voltage (Inv.I/P to non inv.I/P)	±9V
Storage temperature	–55°C to +175°C
Chip operating temperature	+175°C
Operating temperature:	TO – 5 –55°C to +85°C
	DIL –55°C to +125°C

Thermal resistances

Chip-to-ambient:	TO – 5	220°C/W
	DIL	125°C/W
Chip-to-case:	TO – 5	60°C/W
	DIL	40°C/W

PLESSEY
SEMICONDUCTORS

SL500 SERIES
WIDEBAND AMPLIFIERS

SL550 C & D
LOW NOISE WIDEBAND AMPLIFIER WITH EXTERNAL GAIN CONTROL

The SL550 is a silicon integrated circuit designed for use as a general-purpose wideband linear amplifier with remote gain control. At a frequency of 60 MHz, the SL550C noise figure is 1,8dB (typ.) from a 200 ohm source, giving good noise performance directly from a microwave mixer. The SL550 has an external gain control facility which can be used to obtain a swept gain function and makes the amplifier ideal for use either in a linear IF strip or as a low noise preamplifier in a logarithmic strip.

External gain control is performed in the feedback loop of the main amplifier which is buffered on the input and output, hence the noise figure and output voltage swing are only slightly degraded as the gain is reduced. The external gain control characteristic is specified with an accuracy of ±1dB, enabling a well-defined gain versus time law to be obtained.

The input transistor can be connected in common emitter or common base and the quiescent current of the output emitter follower can be increased to enable low impedance loads to be driven.

FEATURES

- 200 MHz Bandwidth
- Low Noise Figure
- Well-Defined Gain Control Characteristic
- 25dB Gain Control Range
- 40dB Gain
- Output Voltage 0.8Vp-p (Typ.)

APPLICATIONS

- Low Noise Preamplifiers
- Swept Gain Radar IFs

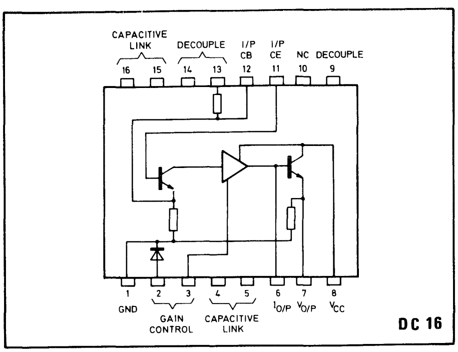


Fig. 1 Pin connections (top view)

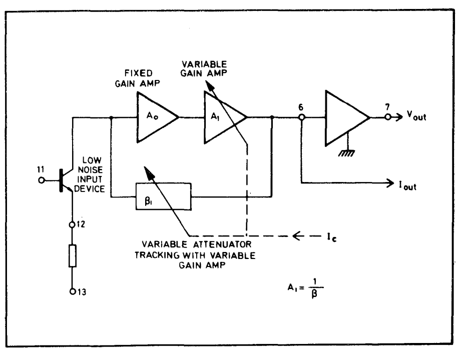


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
f=30MHz $V_S = +6V$, $R_L = 200\Omega$, $I_C = 0$, $R_1 = 750\Omega$, $T_{amb} = +25°C$

Characteristic	Circuit	Value Min.	Value Typ.	Value Max.	Units	Conditions
Voltage gain	SL550C	39	42	44	dB	
	SL550D	35	40	45	dB	
Gain control characteristic	Both		See note 1			
Gain reduction at mid-point	SL550C	9	10	11	db	$I_C = 0.2mA$
	SL550D		9		dB	$I_C = 0.2mA$
Max. gain reduction	SL550C	20	25		dB	$I_C = 2.0mA$
	SL550D		25		dB	$I_C = 2.0mA$
Noise figure	SL550C		2.0	2.7	dB	$R_S = 200\Omega$
	SL550C		3.5		dB	$R_S = 50\Omega$
	SL550D		3.0		dB	$R_S = 200\Omega$
Output voltage	Both		0.15		Vrms	$R_1 = \infty$
	Both		0.3		Vrms	$R_1 = 750\Omega$
Supply current	SL550C		11	13	mA	$R_1 = \infty$
	SL550C		15		mA	$R_1 = 750\Omega$
	SL550D		11	20	mA	$R_1 = \infty$
Gain variation with supply voltage	Both		0.2		dB/V	$V_S = 6$ to 9V
Upper cut-off frequency (—3dB wrt 30MHz)	Both		125		MHz	
Gain variation with temperature (see note 2)	Both		±3		dB	$T_{amb} = -55$ to $+125°C$

NOTES
1. The external gain control characteristic is specified in terms of the gain reduction obtained when the control current (I_C) is increased from zero to the specified current.
2. This can be reduced by using an alternative input configuration (see operating note: 'Wide Temperature Range').

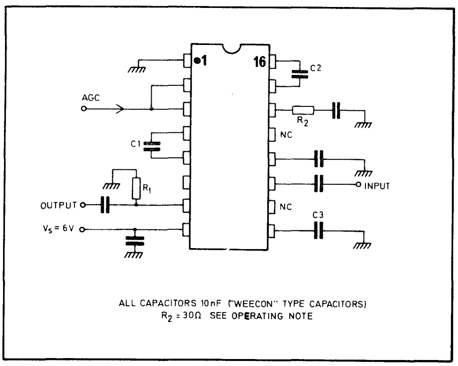


Fig. 3 Test circuit

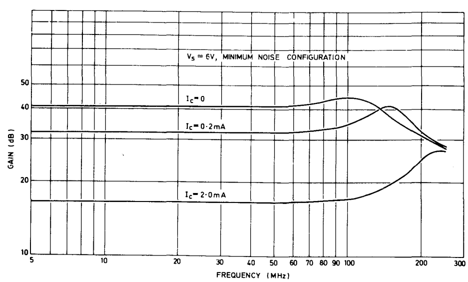


Fig. 4 Frequency response

OPERATING NOTES

Input Impedance

The input capacitance, which is typically 12pF at 60MHz, is independent of frequency. The input resistance, which is approximately 1.5k at 10MHz, decreases with frequency and is typically 500 ohms at 60MHz

Control Input

Gain control is normally achieved by a current into pin 2. Between pin 2 and ground is a forward biased diode and so the voltage on pin 2 will vary between 600 mV at I_C = 1 μA to 800 mV at I_C = 2 mA. The amplifier gain is varied by applying a voltage in this range to pin 3. To avoid problems associated with the sensitivity of the control voltage and with operation over a wide temperature range the diode should be used to convert a control current to a voltage which is applied to pin 3 by linking pins 2 and 3.

Minimum Supply Current

If the full output swing is not required, or if high impedance loads are being driven, the current consumption can be reduced by omitting R_1 (Fig. 3). The function of R_1 is to increase the quiescent current of the output emitter follower.

High Output Impedance

A high impedance current output can be obtained by taking the output from pin 6 (leaving pin 7 open-circuit). Maximum output current is 2 mA peak and the output impedance is 350Ω.

Wide Temperature Range

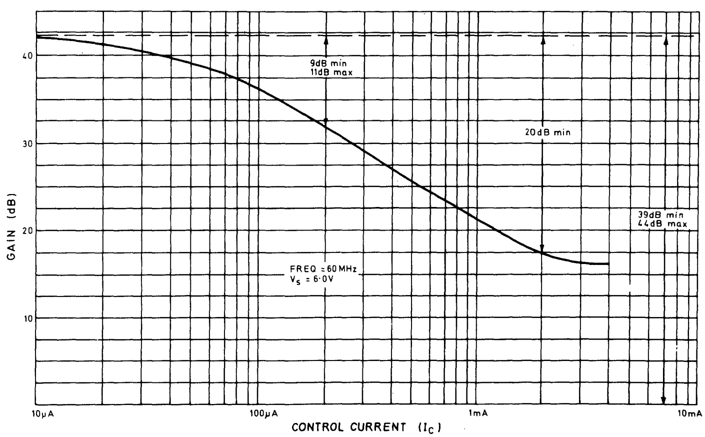
The gain variation with temperature can be reduced at the expense of noise figure by including an internal 30Ω resistor in the emitter of the input transistor. This is achieved by decoupling pin 13 and leaving pin 12 open-circuit. Gain variation is reduced from ±3dB to ±1dB over the temperature range −55°C to +125°C (Figs. 6 and 7)

Low Input Impedance

A low input impedance (≃ 25Ω) can be obtained by connecting the input transistor in common base. This is achieved by decoupling pin 11 and applying the input to pin 12 (pin 13 open-circuit).

High Frequency Stability

Care must be taken to keep all capacitor leads short and a ground plane should be used to prevent any earth inductance common between the input and output circuits. The 30Ω resistor (pin 14) shown in the test circuit eliminates high frequency instabilities due to the stray capacitances and inductances which are unavoidable in a plug-in test system. If the amplifier is soldered directly into a printed circuit board then the 30Ω resistor can be reduced or omitted completely.



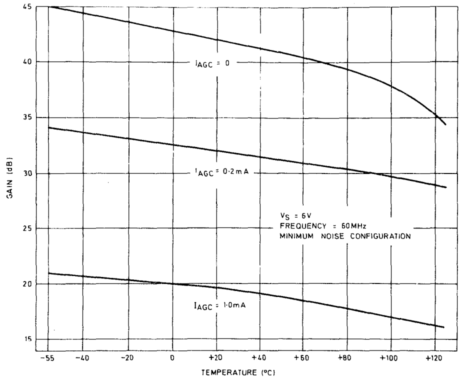


Fig. 6 Voltage gain v. temperature (pin 12 decoupled, standard circuit configuration).

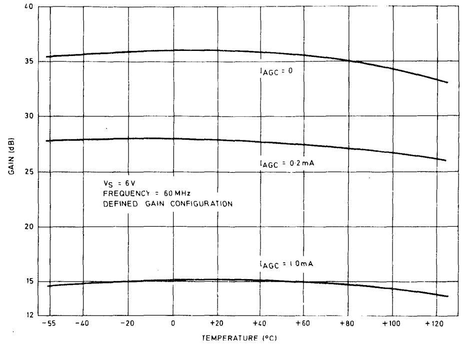


Fig. 7 Voltage gain v. temperature (pin 13 decoupled for improved gain variation with temperature – see operating notes).

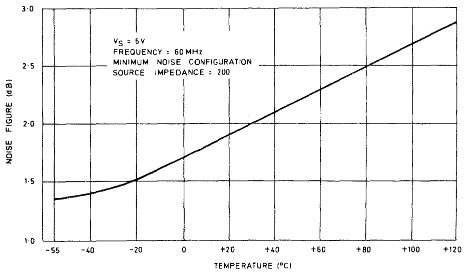


Fig.8 Typical noise figure (SL550C)

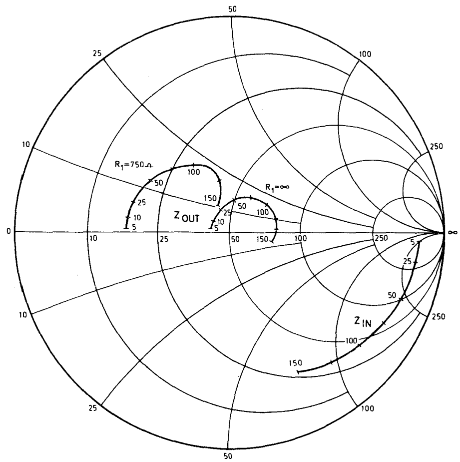


Fig. 9 Input and output impedances (V_S = 6V)

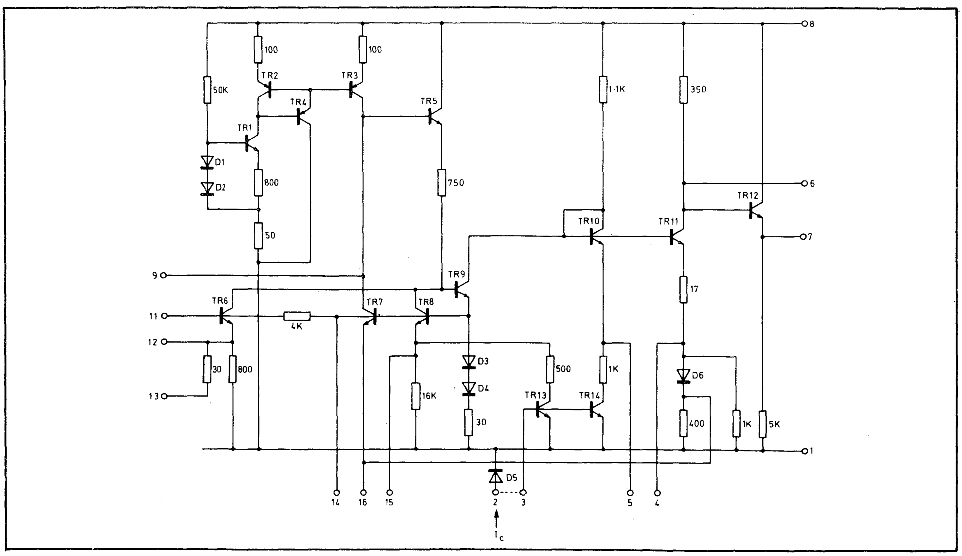


Fig. 10 Circuit diagram

APPLICATION NOTES

A wideband high gain configuration using two SL550s connected in series is shown in Fig. 11. The first stage is connected in common emitter configuration, whilst the second stage is a common base circuit. Stable gains of up to 65 dB can be achieved by the proper choice of R1 and R2. The bandwidth is 5 to 130 MHz, with a noise figure only marginally greater than the 2.0 dB specified for a single stage circuit.

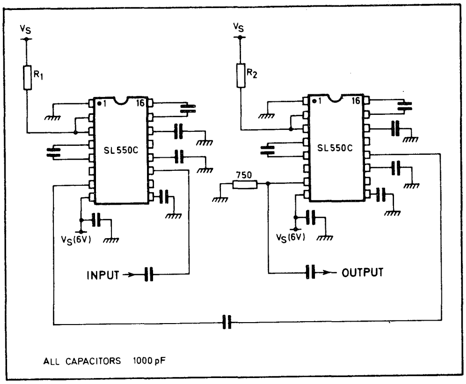


Fig. 11 A two-stage wideband amplifier

A voltage gain control which is linear with control voltage can be obtained using the circuit shown in Fig. 12. The input is a voltage ramp which is negative going with respect to ground. The output drives the control current pins 2 and 3 directly (see Fig. 13). If two SL550s in the strip are controlled as shown in Fig. 14, with a linear ramp input to the linearising circuit, a fourth power law (power gain v. time) will be obtained over a 50 dB dynamic range.

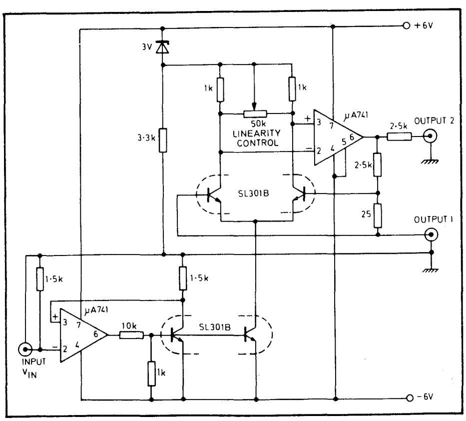


Fig. 12 Gain control linearising circuit.

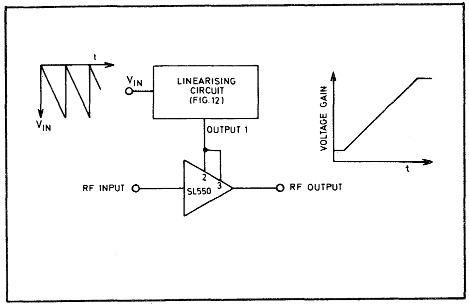


Fig. 13 Linear swept gain circuit

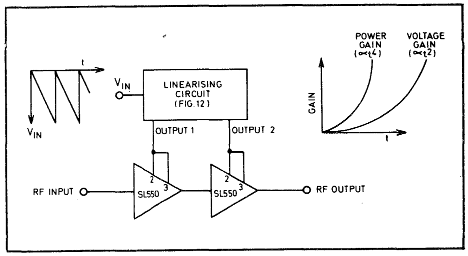
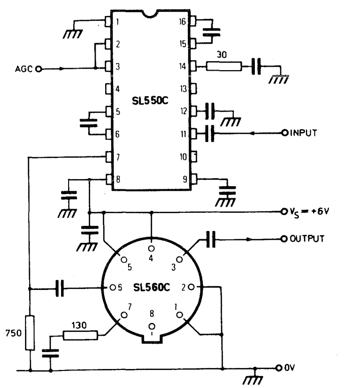


Fig. 14 Square law swept gain circuit.



All capacitors 10nF
Gain 46dB
Noise figure 2.0dB (RS = 200 Ω)
Output power +5dBm (R1 = 50 Ω)
Frequency response as SL550C
Dynamic range 70dB (1MHz bandwidth)

Fig.15 Applications example of wide dynamic range: 50 Ω load amplifier with AGC using SL500 series integrated circuit.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	–55°C to +150°C
Ambient operating temp.	–40°C to +125°C
Max. continuous supply	
Voltage wrt pin 1	+9V
Max. continuous AGC current	
pin 2	10mA
pin 3	1mA

PLESSEY
SEMICONDUCTORS

SL500 SERIES
WIDEBAND AMPLIFIERS

SL560C
300 MHz LOW NOISE AMPLIFIER

This monolithic integrated circuit contains three very high performance transistors and associated biasing components in an eight-lead TO-5 package forming a 300 MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components. The SL 560C is a general-purpose low noise, high frequency gain block.

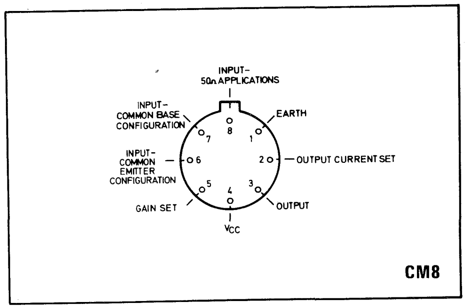


Fig. 1 Pin connections (viewed from beneath)

FEATURES
(Non-simultaneous)

- Gain up to 40 dB
- Noise Figure Less Than 2 dB (R_S 200 ohm)
- Bandwidth 300 MHz
- Supply Voltage 2-15V (Depending on Configuration)
- Low Power Consumption

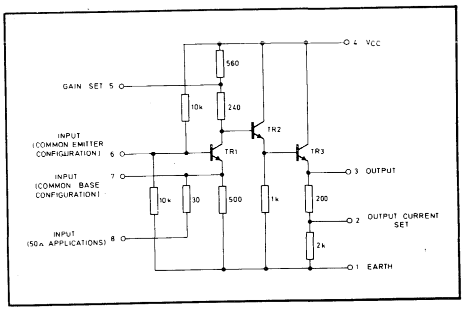


Fig. 2 SL560C circuit diagram

APPLICATIONS

- Radar IF Preamplifiers
- Infra-Red Systems Head Amplifiers
- Amplifiers in Noise Measurement Systems
- Low Power Wideband Amplifiers
- Instrumentation Preamplifiers
- 50 ohm Line Drivers
- Wideband Power Amplifiers
- Wide Dynamic Range RF Amplifiers

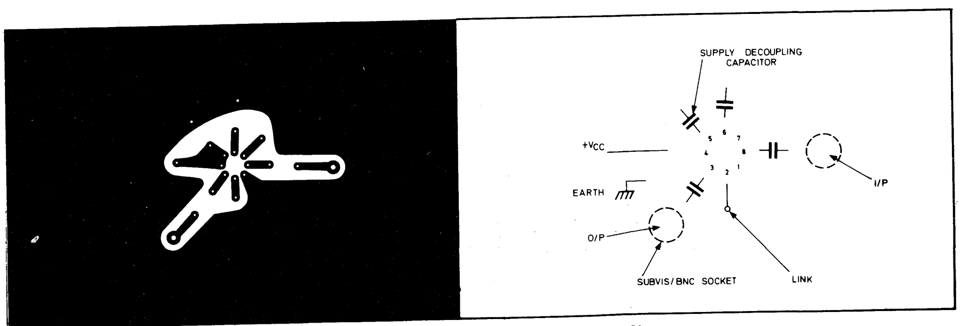


Fig. 3 PC layout for 50- Ω line driver (see Fig. 6)

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Frequency 30 MHz
V_{CC} 6V
$R_S = R_L = 50\Omega$
$T_A = 25°C$
Test Circuit: Fig. 6

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	14	17	dB	
Gain flatness		±1.5		dB	10 MHz — 220 MHz
Upper cut-off frequency		250		MHz	
Output swing	+5	+7		dBM	V_{CC} = 6V } See Fig. 5
		+11		dBm	V_{CC} = 9V } See Fig. 5
Noise figure (common emitter)		1.8		dB	$R_S = 200\Omega$
		3.5		dB	$R_S = 50\Omega$
Supply current		20	30	mA	

CIRCUIT DESCRIPTION

Three high performance transistors of identical geometry are employed. Advanced design and processing techniques enable these devices to combine a low base resistance ($R_{bb'}$) of 17 ohms (for low noise operation) with a small physical size — giving a transition frequency, f_T, in excess of 1 GHz.

The input transistor (TR1) is normally operated in common base, giving a well defined low input impedance. The full voltage gain is produced by this transistor and the output voltage produced at its collector is buffered by the two emitter followers (TR2 and TR3). To obtain maximum bandwidth the capacitance at the collector of TR1 must be minimised. Hence, to avoid bonding pad and can capacitances, this point is not brought out of the package. The collector load resistance of TR1 is split, the tapping being accessible via pin 5. If required, an external roll-off capacitor can be fixed to this point.

The large number of circuit nodes accessible from the outside of the package affords great flexibility, enabling the operating currents and circuit configuration to be optimised for any application. In particular, the input transistor (TR1) can be operated in common emitter mode by decoupling pin 7 and using 6 as the input. In this configuration, a 2 dB noise figure ($R_S = 200\ \Omega$) can be achieved. This configuration can give a gain of 35dB with a bandwidth of 75 MHz (see Figs. 8 and 9) or, using feedback, 14 dB with a bandwidth of 300 MHz (see Figs. 10 and 11).

Because the transistors used in the SL 560C exhibit a high value of f_T, care must be taken to avoid high frequency instability. Capacitors of small physical size should be used, the leads of which must be as short as possible to avoid oscillation brought about by stray inductance. The use of a ground plane is recommended.

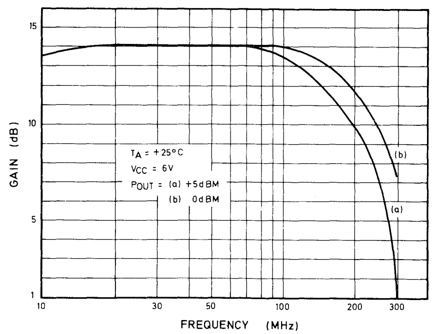


Fig. 4 Frequency response, small signal gain

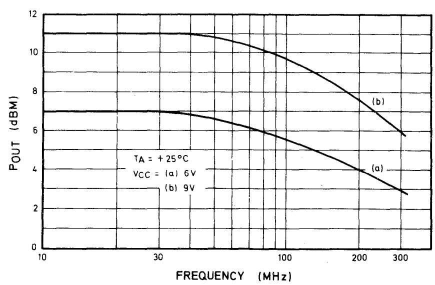
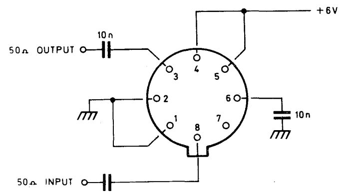


Fig. 5 Frequency response, output capability (loci of maximum output power with frequency, for 1dB gain compression)

TYPICAL APPLICATIONS



Gain 14dB
Bandwidth 220 MHz (P_{out}=1mW, 50 Ω)
200 MHz (P_{out}=5mW, 50 Ω)
Input SWR 1.5:1

Fig. 6 50 Ω line driver. The response of this configuration is shown in Fig. 4.

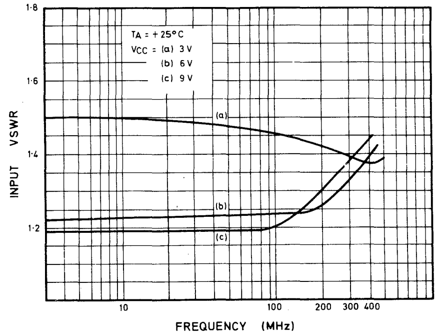
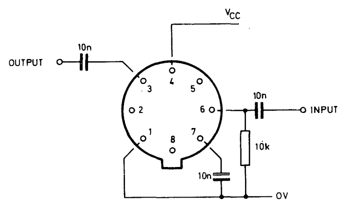


Fig. 7 Input standing wave ratio plot of circuit shown in Fig. 6



Voltage gain 32dB at 6V
35dB at 10V
Noise figure 1.8dB (RS=200 Ω)
Supply current 6mA at 6V
12mA at 10V
Bandwidth 75 MHz (see Fig. 9)

Fig. 8 Low noise preamplifier

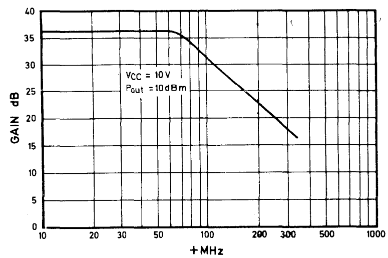
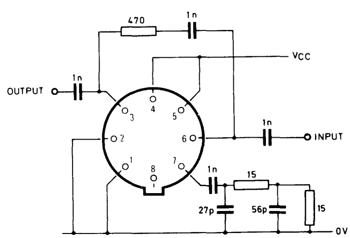


Fig. 9 Frequency response of circuit shown in Fig. 8



Gain 13dB at V_{CC}=9V
—1dB at 6 MHz and 300 MHz

Fig. 10 Wide bandwidth amplifier

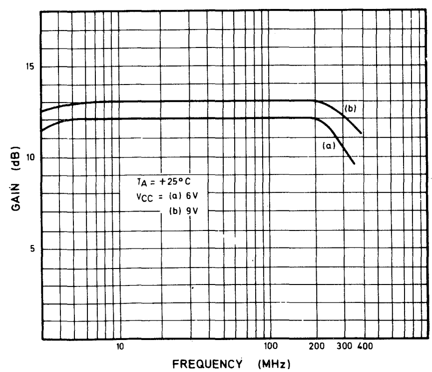


Fig. 11 Frequency response of circuit shown in Fig. 10

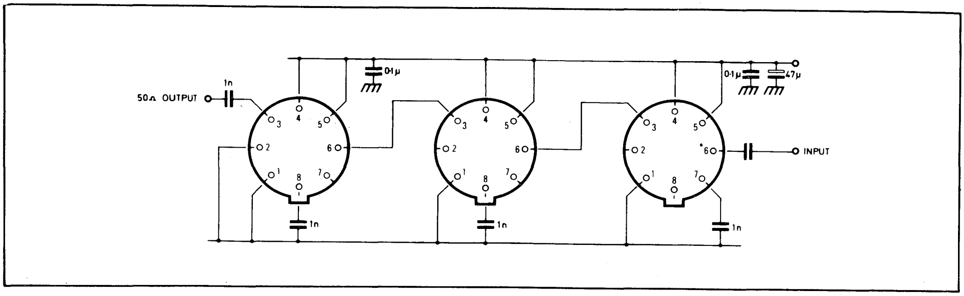


Fig. 12 Three-stage directly-coupled high gain low noise amplifier

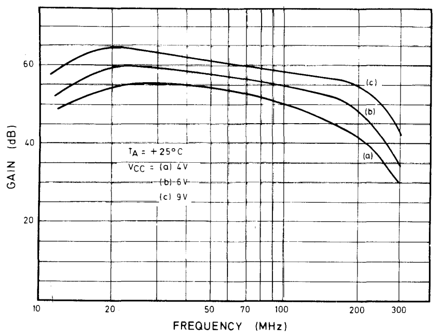
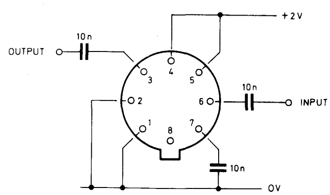


Fig. 13 Frequency response of circuit shown in Fig. 12



Gain 13dB
Power supply current 3mA
Bandwidth 125 MHz
Noise figure 2.5dB (RS=200 Ω)

Fig. 14 Low power consumption amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} (Pin 4 w.r.t. Pin 1)	+15 volts
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +125°C

PLESSEY
SEMICONDUCTORS

SL600 SERIES
COMMUNICATIONS CIRCUITS

SL610C, SL611C & SL612C
RF/IF AMPLIFIERS

The SL610C and SL611C are low noise, low distortion, RF voltage amplifiers with integral supply line decoupling and AGC facilities. The SL610C has a voltage gain of 10 and a bandwidth of 140MHz, while the SL611C has a voltage gain of 20 and a bandwidth of 100MHz. Both circuits have a 50dB AGC range with maximum signal handling of 250mV rms. As they are voltage amplifiers they have high input impedance and low output impedance.

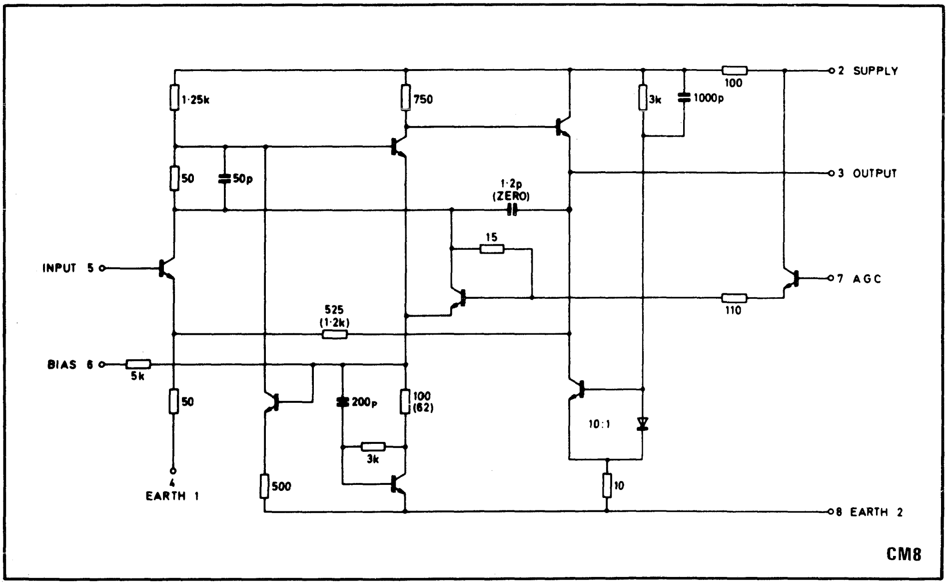


Fig. 1 Circuit diagram of SL610C and SL611C
(Component values in parentheses refer to SL611C)

The SL612C is a low noise, low distortion, IF voltage amplifier similar to the SL610C and SL611C but having a voltage gain of 50, a bandwidth of 15MHz and only 20mW power consumption. It has a 70dB AGC range with maximum signal handling of 250mV rms.

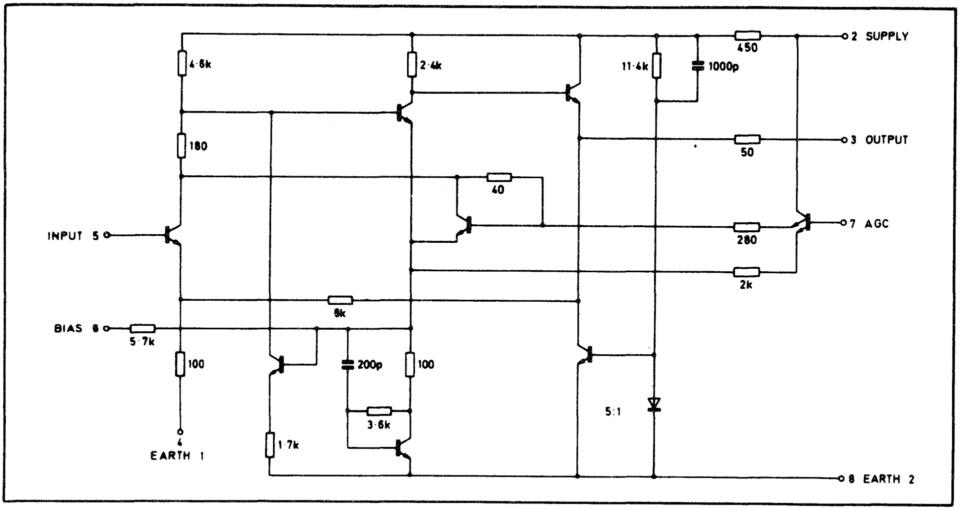


Fig. 2 Circuit diagram of SL612C

ELECTRICAL CHARACTERISTICS

Test conditions: Supply voltage = 6V
Temperature = +25°C (unless otherwise stated)
Pins 5 and 6 strapped together
AGC not applied unless specified.

Characteristic	Circuit	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
Voltage gain	SL610C	18	20	22	dB	30MHz, Source = 25Ω
	SL611C	24	26	28	dB	30MHz, Load R ≥ 500Ω
	SL612C	32	34	36	dB	1.75MHz, Load C ≤ 5pF
Cut-off frequency (−3dB) (See Fig. 9)	SL610C	85	140		MHz	Source = 25Ω
	SL611C	50	100		MHz	Load R ≥ 500Ω
	SL612C	10	15		MHz	Load C ≤ 5pF
Noise Figure	SL610C		4		dB	Source = 300Ω, f = 30MHz
	SL611C		4		dB	Source = 300Ω, f = 30MHz
	SL612C		3		dB	Source = 800Ω, f = 1.75MHz
Max. input signal (1% cross modulation) No AGC applied	SL610C		100		mVrms	Load 150Ω, f = 10MHz
	SL611C		50		mVrms	Load 150Ω, f = 10MHz
	SL612C		20		mVrms	Load 1.2kΩ, f = 1.75MHz
Max. input signal (1% cross modulation) Full AGC applied	SL610C		250		mVrms	f = 10MHz
	SL611C		250		mVrms	f = 10MHz
	SL612C		250		mVrms	f = 1.75MHz
AGC range (See Fig. 10)	SL610C	40	50		dB	
	SL611C	40	50		dB	
	SL612C	60	70		dB	
AGC current	SL610C		0.15	0.6	mA	
	SL611C		0.15	0.6	mA	AGC Voltage = 5.1V
	SL612C		0.15	0.3	mA	
Quiescent current consumption	SL610C		15	20	mA	
	SL611C		15	20	mA	Output open circuit
	SL612C		3.3	5	mA	
Change of voltage* gain with temperature	All types		±1		dB	−55°C to +125°C
Change of AGC range* with temperature	All types		±2		dB	−55°C to +125°C
*from nominal						

Gain and frequency response of these circuits are relatively independent of supply voltage within the range 6 – 9V

OPERATING NOTES

The SL610C, SL611C and SL612C are normally used with pins 5 and 6 strapped. A slight improvement in noise figure, and an increase in the LF input impedance may be obtained by making the necessary AC connection via the earthy end of an input tuned circuit in the conventional manner.

The characteristics of these units have been expressed in G parameters which are defined as shown in Fig. 3.

These parameters correspond to the normal operation of a voltage amplifier which is usually operating into a load much higher than its output impedance and from a source much lower than its input impedance. Hence the input admittance (G_{11}) and voltage gain (G_{21}) are measured with open circuit output, and the output impedance (G_{22}) with short circuit input. The parasitic feedback parameter is the current transfer (G_{12}) i.e. the current which flows in a short circuit across the input for a given current flowing in the output circuit.

Since the effects of G_{12} are small for reasonable values of load and source impedance, the approximate equivalent circuit given in Fig. 4 may be used.

Hence the typical effects of applying finite load and source impedances, real or complex, may be evaluated by the use of the graphs showing the values of the major parameters versus frequency. At lower frequencies the limitation on Z_L is dependent upon output signal; for maximum output $Z_L = 100\Omega$.

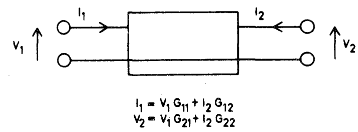


Fig. 3 Definition of G parameters

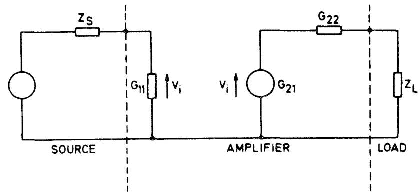


Fig. 4 Amplifier equivalent circuit

Stability

Both the input admittance G_{11} and the output impedance G_{22} have negative real parts at certain frequencies. The equivalent circuits of input and output respectively are shown in Fig. 5 and 6 and the values of R_{in}, R_{out}, C_{in} and L_{out} may be determined for any particular frequency from the graphs Fig. 7 and 8. It will be seen that, for the SL610C and the SL611C R_{in} is negative between 30 and 100MHz, and R_{out} is negative over the whole operating frequency range. For the SL612C, R_{in} is not negative and R_{out} is negative only below 700KHz.

It is evident that if an inductive element having inductance L1 and parallel resistance R1 is connected across the input, oscillation will occur if R_{in} is negative at the resonant frequency of C_{in} and L1, and R1 is higher than R_{in}.

Similarly, if a capacitor C1 in series with a resistance R2 is connected across the output oscillation will occur if, at the resonant frequency of L_{out} and C1, R_{out} has a negative resistance greater than the positive resistance R2. Where the input may be inductive, therefore, it may be shunted by a resistor and where the load may be capacitive 47Ω should be placed in series with the output.

These devices may be used with supplies up to +9V with increased dissipation.

The AGC characteristics shown in Fig. 8 vary somewhat with temperature: a preset potentiometer should not, therefore, be used to set the gain of either of these circuits if gain stability is required.

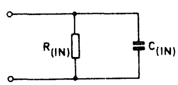


Fig. 5 Input circuit

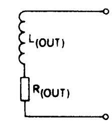


Fig. 6 Output circuit

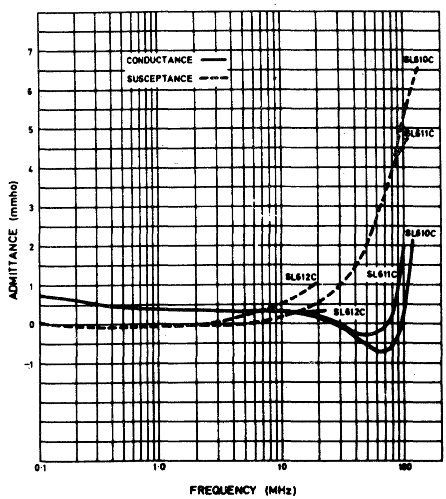


Fig. 7 Input admittance with o/c output (G_{11})

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +150°C
Operating temperature range	−55°C to +125°C
Chip-to-ambient thermal resistance	220°C/W
Chip-to-case thermal resistance	60°C/W
Supply voltage	12V

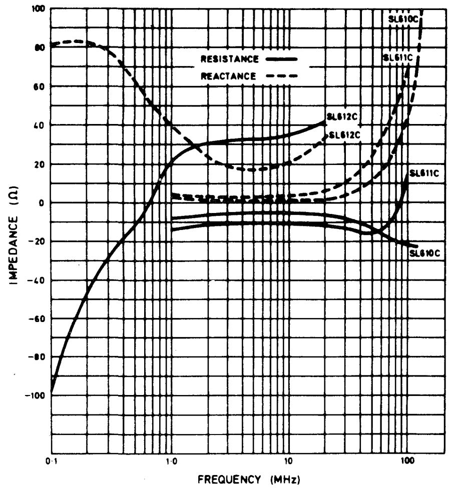


Fig. 8 Output impedance with s/c input (G_{22})

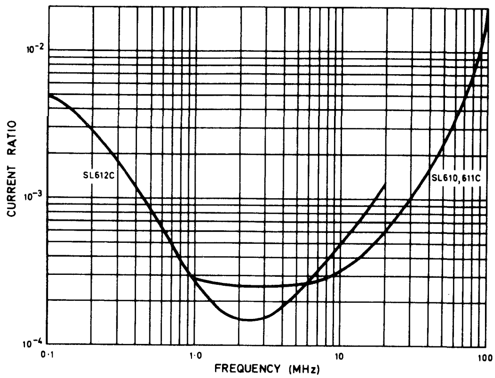


Fig. 11 Reverse current transfer ratio (G_{12})

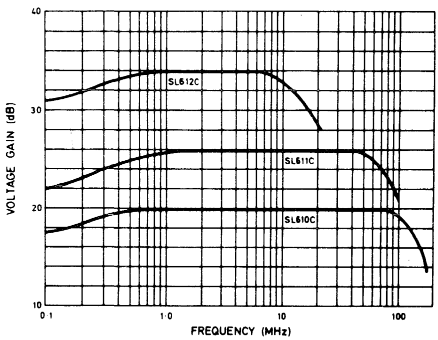


Fig. 9 Voltage gain (G_{21})

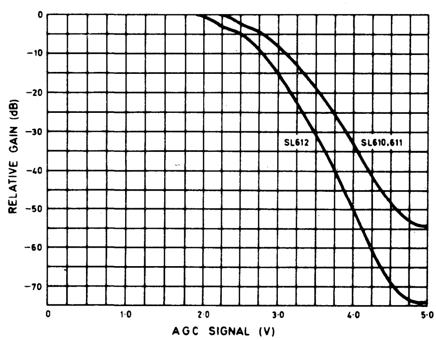


Fig. 10 AGC characteristics

TYPICAL MAX. FREE AIR OPERATING TEMPERATURES (°C)

Supply Voltage	6V		9V		12V	
AGC Voltage	None	Full	None	Full	None	Full
SL610C/611C	153	129	118	58	–	–
SL612C	171	158	165	129	149	69

PLESSEY SEMICONDUCTORS

SL600 SERIES
COMMUNICATIONS CIRCUITS

SL613C
LIMITING AMPLIFIER/DETECTOR

The SL613C is a low noise limiting amplifier intended for use as an RF clipper, a limiting stage in IF amplifiers, or an RF Compressor in SSB transmitters. It contains a detector which may be used to detect AM but is particularly intended for use as an AGC detector. The amplifier, which has a gain of 12 dB when not limiting, has upper and lower 3 dB points of 150 MHz and 5 MHz respectively. It limits when its input exceeds 120 mV r.m.s. The detected output during limiting is 1 mA.

FEATURES

- Wide Bandwidth
- Low Noise
- Highly Symmetrical Limiting
- Large Signal Handling Capability

APPLICATIONS

- RF Clippers
- AGC Systems
- AM Detectors
- RF Compression in SSB Transmitters

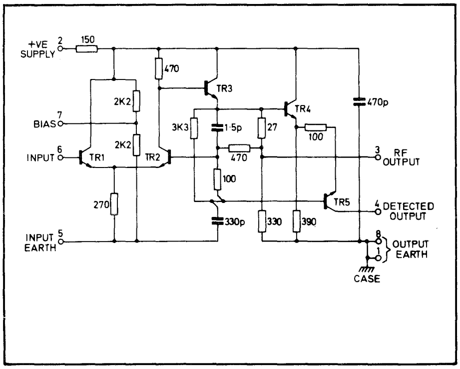


Fig. 1 Circuit diagram

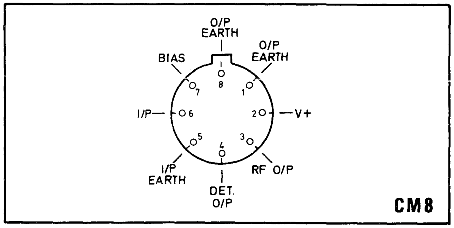


Fig. 2 Pin connections

ELECTRICAL CHARACTERISTICS

Test Conditions
Supply +6V
Temperature +25°C
Pins 6 & 7 strapped together

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	3.3	4	4.6	–	30 MHz
Upper 3 dB frequency	120	150		MHz	
Lower 3 dB frequency		5	8	MHz	
Noise figure		4.5	5.5	dB	60 MHz 500Ω source
Supply current	11	15	20	mA	No signal
Limited RF o/p		1.25		V p-p	0.5 V input, 30 MHz
Detector current	0.85	1	1.25	mA	0.5 V input, 30 MHz
Maximum input before overload	1.5	1.75		V r.m.s.	30 MHz
Input impedance		5kΩ + 6pF			60 MHz. Open circuit o/p

OPERATING NOTES

The SL613C, like the SL610/11/12, is normally used with the input and bias pins connected directly together and the input applied through a capacitor. However, and again like the SL610/11/12, the bias may be decoupled and connected to the 'cold' end of a coil or tuned circuit, the input pin being connected to its 'hot' end or to a tap.

The supply rail is decoupled internally at RF but as the gain is dependent on supply voltage there should no appreciable LF ripple on the supply. Two separate earth connections are made in order to minimise the effects of common earth-lead inductance – such common earth-lead inductance can cause instability and care should be taken not to introduce it externally.

The RF output is capable of driving a load of 1kΩ in parallel with 10pF. If a capacitive load of more than 10pF is envisaged a resistor should be connected between the output pin and the load. Normally 50Ω is sufficient. The output should be isolated at DC by a capacitor.

The detected output consists of a current out of pin 4, which is an NPN transistor collector. This pin must always be more than 3 volts more positive than earth, even if the detected output is not required (in which case it is best to strap pins 2 and 4).

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30°C to +85°C
Operating temperature	−30°C to +70°C
Supply voltage (pins 2 or 4)	+9V

PLESSEY
SEMICONDUCTORS

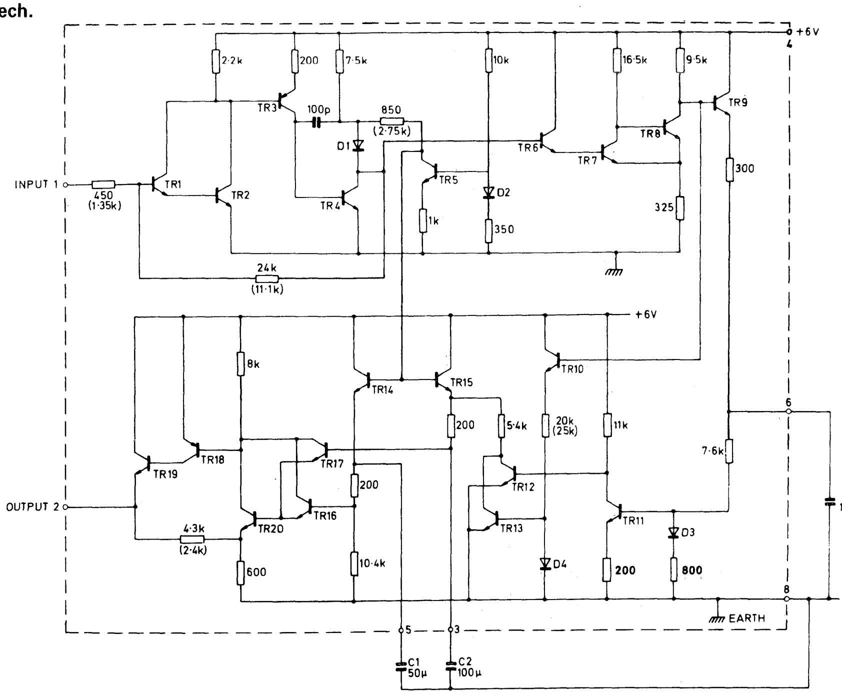
SL600 SERIES
COMMUNICATIONS CIRCUITS

SL620C & SL621C
AGC GENERATORS

The SL621C is an AGC generator designed specifically for use in SSB receivers in conjunction with the SL610C, SL611C and SL612C RF and IF amplifiers. In common with other advanced systems it generates a suitable AGC voltage directly from the detected audio waveform, provides a 'hold' period to maintain the AGC level during pauses in speech, and is immune to noise interference. In addition it will smoothly follow the fading signals characteristic of HF communication.

When used in a receiver comprising one SL610C and one SL612C amplifier and a suitable detector, the SL621C will maintain the output within a 4dB range for a 110dB range of receiver input signal.

The SL620C VOGAD (Voice Operated Gain Adjusting Device) is an AGC generator designed to work in conjunction with the SL630C audio amplifier (particularly when the latter is used as a microphone amplifier) to maintain the amplifier output between 70mV and 87mV rms for a 35 dB range of input. A one second 'hold' period is provided which prevents any increase of background noise during pauses in speech.



CM8

Fig. 1 Circuit diagram of SL620C and SL621C (Component values in brackets refer to SL620C)

DESCRIPTION

The operation of the SL621C is described with reference to the circuit diagram, Fig. 1, and Fig. 2 which illustrates the dynamic response of a receiver controlled by the SL621C.

The SL621C consists of an input AF amplifier TR1 – TR4 (3 dB point: 10KHz) coupled to a DC output amplifier, TR16 – TR19, by means of a voltage back-off circuit, TR5 and two detectors, TR14 and TR15, having short and long rise and fall time constants respectively.

The detected audio signal at the input will rapidly establish an AGC level, via TR14, in time t_1 (see Fig. 2). Meanwhile the long time constant detector output will rise and after t_3 will control the output because this detector is the more sensitive.

If signals exist at the SL621C input which are greater than approximately 4mV rms they will actuate the trigger circuit TR6 – TR8 whose output pulses will provide a discharge current for C2 via TR10, TR13.

By this means the voltage on C2 can decay at a maximum rate, which corresponds to a rise in receiver gain of 20 dB/s. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However, should the receiver input signals fade faster than this, or disappear completely as during pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector will drop to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C3 via TR9, so holding off TR12 via TR11. When the trigger pulses cease, C3 discharges and after t_5 turns on TR12. Capacitor C2 is discharged rapidly (in time t_4) via TR12 and so full receiver gain is restored. The hold time, t_5 is approximately one second with C3 = 100μF. If signals reappear during t_5, then C3 will re-charge and normal operation will continue. The C3 re-charge time is made long enough to prevent prolongation of the hold time by noise pulses.

Fig. 2 shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

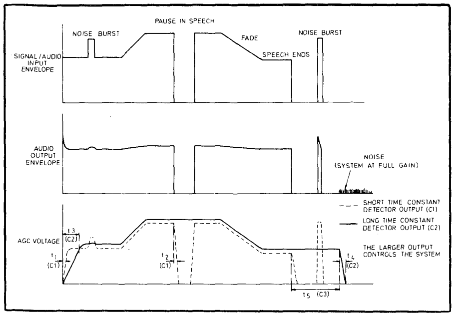


Fig. 2 Dynamic response of a system controlled by SL620C or SL621C AGC generator

OPERATING NOTES

The various time constants quoted are for C1 = 50μF and C2 = C3 = 100μF. These time constants may be altered by varying the appropriate capacitors.

An input coupling capacitor is required. This should normally be 0.33μF for an SL621C and about 1μF for an SL620C.

Fig. 3 shows how the SL621C may be connected into a typical SSB receiver.

Fig. 4 shows how the SL620C is used to control the gain of the SL630C audio amplifier. The operation of the SL620C is exactly the same as that of the SL621C and the diagram showing the dynamic response of the closed loop system, Fig. 2, is equally applicable to the SL630C/SL620C combination. Again, the time constants may be altered by varying the capacitor values.

The supply must either have a source resistance of less than 2Ω at LF or be decoupled by at least 500μF so that it is not affected by the current surge resulting from a sudden input on pin 1. The devices may be used with a supply of up to +9V.

In a receiver for both AM and SSB using an SL623C detector/Carrier AGC generator, the AGC outputs of the SL621C and SL623C may be connected together provided that no audio reaches the SL621C input while the SL623C is controlling the system.

AGC lines may require some RF decoupling but the total capacitance on the output of an SL620 or SL621 should not exceed 15000pF or the impulse suppression will suffer.

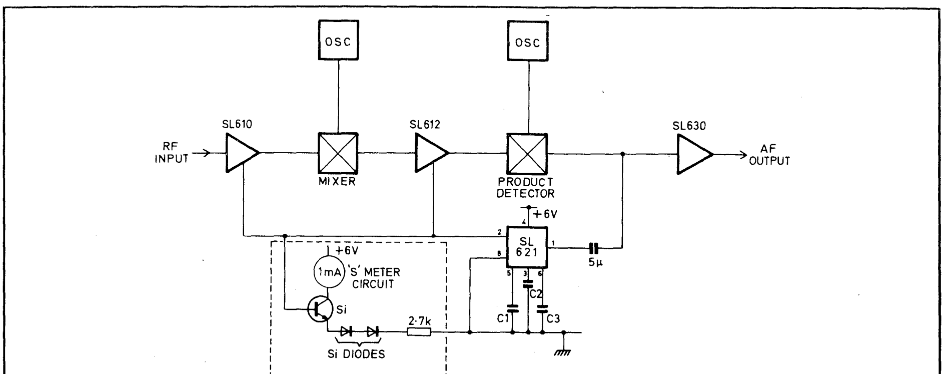


Fig. 3 SL621C used to control SSB receiver

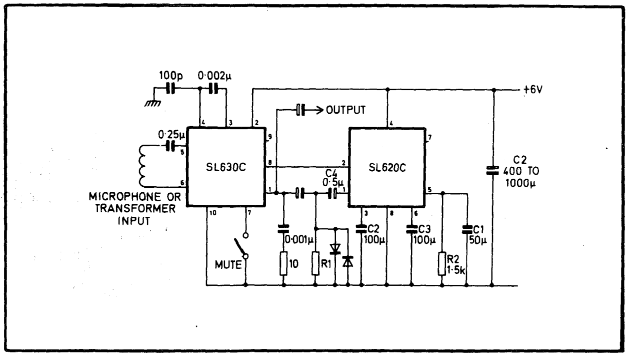


Fig. 4 SL620C used to control SL630C audio amplifier

ELECTRICAL CHARACTERISTICS SL 620C & SL 621C

Test conditions: Supply voltage = 6V
Temperature = +25°C
Input signal frequency = 1kHz

Characteristic	Circuit	Value				Test Conditions
		Min.	Typ.	Max.	Units	
Input for 0.65V dc output	SL620C	55	70	85	mVrms	See Fig.5 (Measurement accuracy 1 dB)
Input for 1.5V dc output	SL620C	70	87	105	mVrms	See Fig.5 (Measurement accuracy 1 dB)
Input for 2.2V dc output	SL621C	6.0	7.0	10.0	mVrms	See Fig.6 (Measurement accuracy 1 dB)
Input for 4.6V dc output	SL621C	9.0	11.0	16.0	mVrms	See Fig.6 (Measurement accuracy 1 dB)
*Fast rise time, t_1	Both		20	30	ms	0–50% full output (C_1 = 50μF)
*Fast decay time, t_2	Both	150	200	250	ms	100%–36% voltage on C_1 (C_1 = 50μF)
*Slow rise time, t_3	Both	150	200	300	msec	Time to output transition point (C_2 = 100μF)
Input 3 dB point	Both		10		kHz	(C_2 = 100μF)
Maximum fade rate	SL620C		0.22		V/s	(C_2 = 100μF)
	SL621C		0.45		V/s	(C_2 = 100μF)
*Hold collapse time, t_4	Both	150	200	250	ms	Full-zero output (C_2 = 100μF)
*Hold time, t_5	Both	0.75	1.0	1.25	s	C_3 = 100μF
A.C. ripple on output	Both		12	20	mVp-p	1kHz. Output open circuit
Maximum output voltage	SL620C	2.0			V	
	SL621C	5.1			V	
Quiescent current consumption	Both	2.5	3.1	4.1	mA	
Surge current	Both		30		mA	
Input resistance	SL620C	1	1.4	2	kΩ	
	SL621C	350	500	700	Ω	
Output resistance	SL620C	12	40	130	Ω	
	SL621C	20	70	230	Ω	

**See Figure 2*

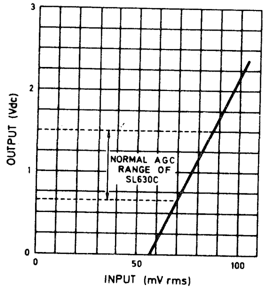


Fig. 5 Transfer characteristic of SL620C

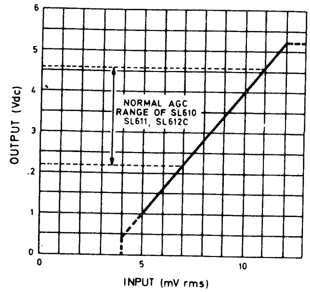


Fig. 6 Transfer characteristic of SL621C

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Free air operating temperature	−25°C to +125°C
Chip-to-ambient thermal resistance	220°C/W
Chip-to-case thermal resistance	60°C/W
Supply voltage	12V

PLESSEY
SEMICONDUCTORS

SL600 SERIES
COMMUNICATIONS CIRCUITS

SL622C
AF AMPLIFIER, VOGAD & SIDETONE AMPLIFIER

The SL622C is a silicon integrated circuit combining the functions of audio amplifier with voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low-sensitivity microphone and to provide an essentially constant output signal for a 60 dB range of input.

Additionally, a constant gain amplifier is incorporated which provides an amplitude-limited output for sidetone in mobile transmitter/receiver applications.

The encapsulation is a 10 lead TO-5 package and the device is designed to operate from a 6 to 12 volt supply, over a temperature range of −55°C to +125°C.

A voltage regulator produces an independent supply line at 4.7 Volts stabilised

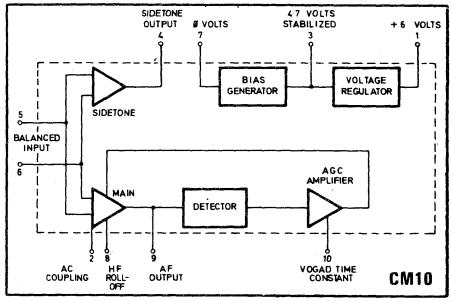


Fig. 1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test Conditions: Input frequency 1KHz
Supply voltage +6V
Temperature +25°C

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
VOGAD output level	55	90	110	mV rms	Balanced signal input 18mV rms
Sidetone output level	600	800	900	mV p-p	Balanced signal input 18mV rms
AF amplifier voltage gain	49	52	55	dB	Balanced signal input 72μV rms
Sidetone voltage gain	24.5	29	30.5	dB	Balanced signal input 72μV rms
Current consumption consumption		14	16	mA	6V supply, input 1mV rms
		24		mA	12V supply, input 1mV rms
Decay time – time for VOGAD output to return to within 10% of original absolute level when signal input voltage is switched down 20dB.		1.0		s	Original balanced signal input 18mV rms; R1 = 1 MΩ, C3 = 47μF, Test cct. as Fig.2
Attack time – time for VOGAD output to return to within 10% of original absolute level when signal input voltage is switched up 20dB.		20		ms	Original balanced signal input 1.8mV rms; R1 = 1 MΩ, C3 = 47μF, Test cct. as Fig.2
Total harmonic distortion at VOGAD output.		2		%	Balanced signal input 90mV rms
Differential input impedance.		300		Ω	
Single-ended input impedance.		180		Ω	
Sidetone output impedance		200		Ω	
AF amplifier output resistance		50		Ω	
VOGAD operating threshold (Whisper threshold)		100		μV rms @ I/P	

T5▷

OPERATING NOTES

The SL622C incorporates a series regulator which will accept supply voltages between 6V and 12V and provides a supply line rejection of approximately 26 dB when operated from a 6V supply The supply line immunity increases with supply voltage.

The input stage is a differential class A-B stage with an AGC terminal. The accurate balance of the input stage give an overall common-mode rejection ratio of greater than 30 dB.

Typically the amplifier will handle differential input signals of up to 375mV p-p and unbalanced signals of up to 50mV p-p. When used in the unbalanced mode either pin 5 or pin 6 may be used as the input, the other being decoupled to earth.

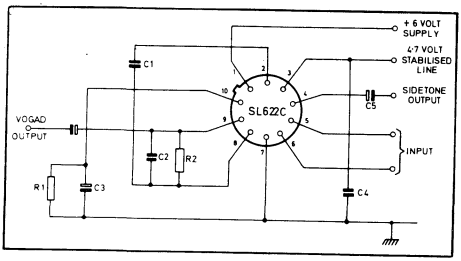


Fig. 2 Connection diagram for SL622C used as a microphone amplifier.

Fig. 2 shows the SL622C when used as a balanced microphone amplifier. The LF cut-off of the amplifier is set by C1 – and also by the values of coupling capacitors to the input pins (pin 5 and pin 6); coupling capacitors should be used if the d.c. potential of the input is not floating with respect to earth.

The HF cut-off is set by C2. The VOGAD threshold may be increased by connecting an external conductance between pins 8 and 9. The threshold is increased by approximately 20 dB for 1 millimho of conductance, the value of C2 should be adjusted in conjunction with any threshold alteration in order to obtain the desired bandwidth.

C3 and R1 set the attack and decay rates of the VOGAD. C3 = 47μF and R1 = 1Mohm gives an attack time constant (gain increasing) of 20 millisecs and a decay rate of 20 dB/sec. C1 = 2.2μF and C2 = 4.7nF give a 3 dB bandwidth of approximately 300Hz to 3kHz.

The amplifier can be muted by applying +4V to pin 10, but when the voltage is removed either C3 must be discharged or there will be an appreciable delay before the circuit functions normally again.

C4 is used for RF decoupling of the stabilised line. AF decoupling may be applied to improve supply line rejection and sidetone linearity.

The VOGAD and sidetone steady-state transfer characteristics are shown in Figs. 3 and 4.

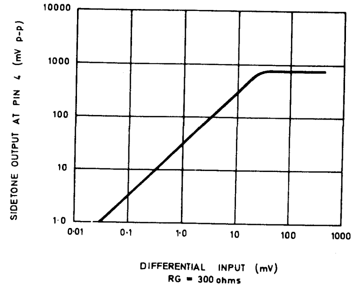


Fig. 3 Sidetone output characteristics.

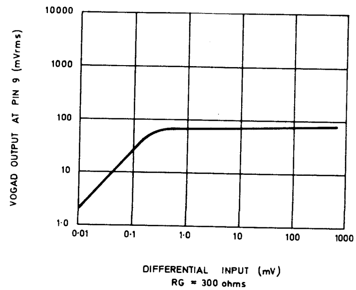


Fig. 4 VOGAD – output characteristics (1kHz sinewave input).

Pin	Function
1	+6 volts supply
2	A.C. coupling
3	+4.7V decoupling
4	Sidetone o/p
5, 6	Balanced signal input
7	OV
8	HF Roll off
9	AF o/p
10	VOGAD time constant.

ABSOLUTE MAXIMUM RATINGS

Continuous supply voltage (positive)	12V ± 0.5V
Storage temperature	–55°C to + 175°C
Ambient temperature (6V operating)	–55°C to + 125°C
(12V operating)	–55°C to + 100°C

PLESSEY
SEMICONDUCTORS

SL600 SERIES
COMMUNICATIONS CIRCUITS

SL623C

AM DETECTOR, AGC AMPLIFIER & SSB DEMODULATOR

The SL623C is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator with SSB demodulator. It is designed specially for use in SSB/AM receivers in conjunction with SL610C, SL611C and SL612C RF and IF amplifiers. It is complementary to the SL621C SSB AGC generator.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL610C and one SL612C amplifier, the SL623C will maintain the output within a 5 dB range for a 90 dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100 mV, contributes negligible distortion up to 90% modulation. The SSB demodulator is of single balanced form. The SL623C is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies. The encapsulation is a 10 lead TO-5 package and the device is designed to operate from a 6 volt supply, over a temperature range of −55°C to +125°C.

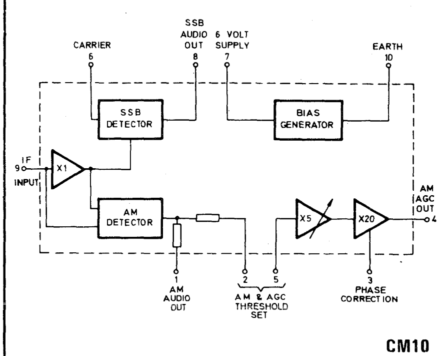


Fig. 1 Block Diagram

ELECTRICAL CHARACTERISTICS @ SUPPLY = +6V, T_{amb} = + 25°C

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
SSB Audio Output	25	30	42	mV rms	Signal Input 20mV rms @ 1.748 MHz. Ref. Signal Input 100mV rms @ 1.750 MHz
AM Audio Output	45	55	64	mV rms	Signal Input 125mV rms @ 1.75 MHz. Modulated to 80% @ 1 kHz.
AGC Range (change in input level to increase AGC output voltage from 2.0V to 4.6V)			5	dB	Initial signal input 125mV rms at 1.75 MHz. Mod. to 80% at 1 kHz Output Set with 10k Ω pot between pins 2 & 5 to 2.0V.
Quiescent Current Consumption		9	11	mA	Output open circuit
Max. operating frequency		30		MHz	
Change of SSB audio output with temperature +85°C		−0.5		dB	Signal Input 20mV rms @ 1.784 MHz. Ref. signal input 100mV rms @ 1.75 MHz.
−40°C		+0.5		dB	
Change of AM audio output with temperature +85°C		−0.25		dB	Signal Input 125mV rms @ 1.75 MHz Modulated to 80% @ 1 kHz.
−40°C		−0.25		dB	

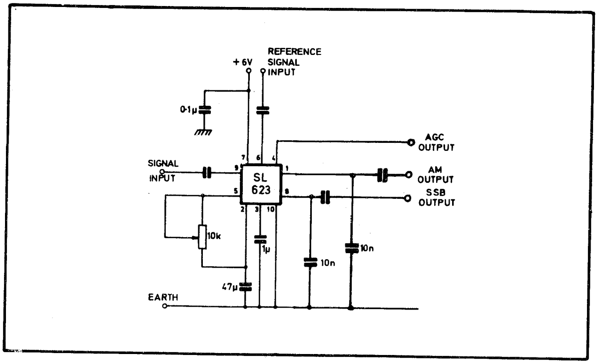


Fig. 2 Typical circuit using the SL623C as signal detector and AGC generator.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Ambient operating temperature	−55°C to +125°C
Supply voltage	−0.5V to +12V

PLESSEY SEMICONDUCTORS

SL600 SERIES
COMMUNICATIONS CIRCUITS

SL624C

MULTIMODE DETECTOR

The SL624C is a complex integrated circuit designed for use as a detector of AM, FM, SSB or CW, acting respectively as a synchronous detector, a quadrature detector and a product detector with built-in oscillator. It also contains a voltage-controlled gain system and a separate audio amplifier capable of driving a single transistor output stage.

A major advantage of the SL624C as an AM detector is that unlike an envelope detector, it does not give an output on broad band IF noise when used in a typical receiver following a block filter and a broadband IF amplifier.

FEATURES

- Demodulates FM, AM, SSB and CW
- Operates up to 30 MHz (Typ)
- Voltage-Controlled Audio Gain
- Separate Audio Driver

APPLICATIONS

- Mobile Transceivers
- HF Transceivers
- VHF Transceivers

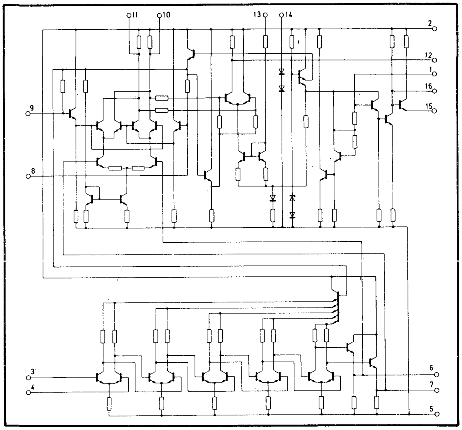


Fig. 1 Circuit diagram

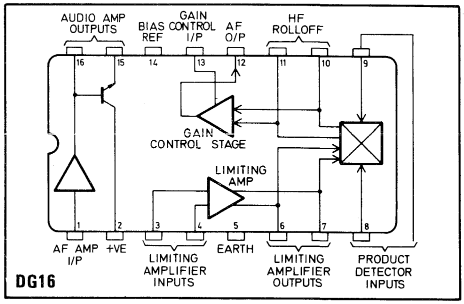


Fig. 2 Block diagram and pin connections (top)

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply +12V
Temperature +25°C (unless otherwise stated)

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply voltage	9	12	15	V	
Current drain		23		mA	
Minimum input for synchronous AM detector					
+25°C		1		mV r.m.s.	9 MHz input
−55°C to +125°C		5			
Minimum input for limiting					
+25°C		100		μV r.m.s.	9 MHz input
−55°C to +125°C		300			
Detector audio gain range		80		dB	
Audio amplifier input R	20	50		kΩ	
Audio amplifier voltage gain		4		–	
Maximum operating frequency (limiting amplifier)		30		MHz	

OPERATING NOTES

Figs. 3, 4 and 5 show the SL624C used, respectively, as a synchronous AM detector, a quadrature FM detector and a self-oscillating product detector. It is evident that a multimode receiver may be made either by switching the components around one SL624C with relays or diodes, or by using three SL624Cs, one per mode.

The supply to the SL624C should be decoupled at HF by a 0.1 μF capacitor sited as near as possible to pins 2 and 5.

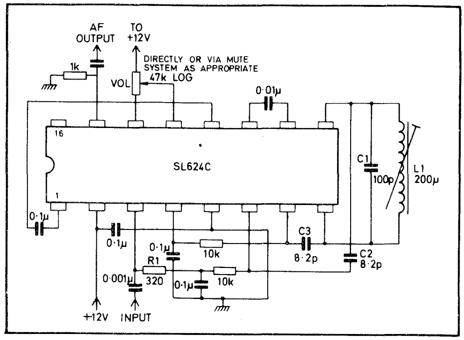


Fig. 4 FM quadrature detector

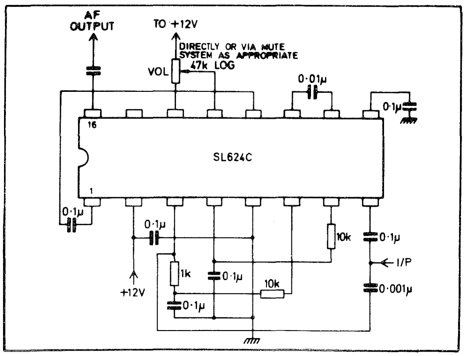


Fig. 3 Synchronous AM detector

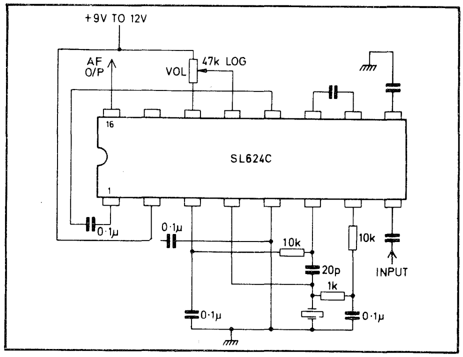


Fig. 5 Self-oscillating product detector

ABSOLUTE MAXIMUM RATINGS

Storage temperature:	–55°C to +150°C.
Operating temperature:	–55°C to +125°C.
Supply voltage (pin 2):	+18V.

PLESSEY SEMICONDUCTORS

SL600 SERIES
COMMUNICATIONS CIRCUITS

SL630C

MICROPHONE/HEADPHONE AMPLIFIER

The SL630C is designed specifically for use as a microphone or headphone amplifier. It has a voltage gain of 100, will accept balanced or unbalanced inputs, and can deliver up to 250mW output from a class AB push-pull output stage.

A gain control facility with a logarithmic law allows a.g.c. to be applied when the device is used as a microphone amplifier, and also allows remote volume control with a linear potentiometer. Gain reduction of 100 dB may be obtained

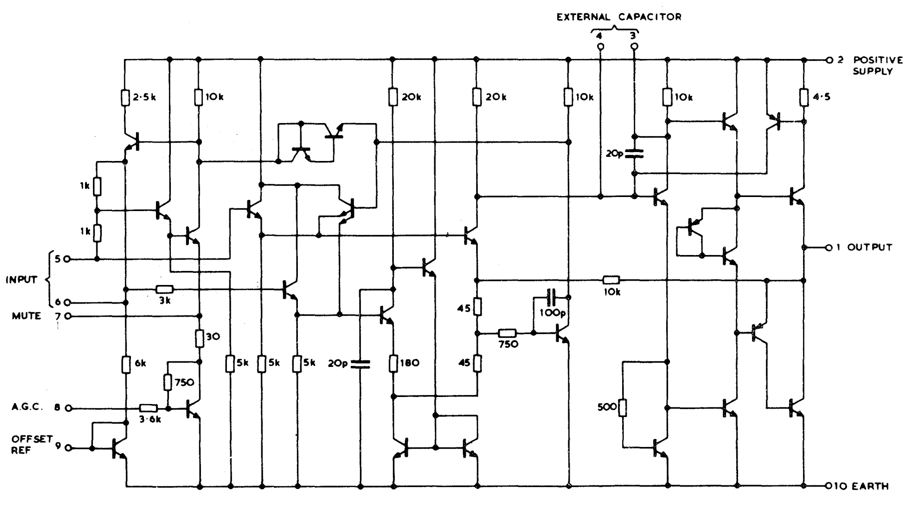


Fig 1 Circuit diagram

CM10

ELECTRICAL CHARACTERISTICS

Test conditions: Temperature = +25°C
Signal Frequency = 1kHz
Supply = 12V (unless otherwise stated)

Characteristic	Value			Units	Test Conditions
	Min.	Typ.	Max.		
Differential input voltage gain	38	40	42	dB	Input 1mVrms
Single ended input voltage gain	43	46	49	dB	Input 1mVrms
Maximum output voltage		1.2		Vrms	6V supply
	2.5	2.8		Vrms	12V supply
Maximum output power		See Fig. 6			0.5% distortion
Quiescent current (See also Fig. 6)			5	mA	6V supply
			13	mA	12V supply
Differential input impedance	1.0	2.0	3.6	kΩ	
Single ended input impedance		1.0	1.8	kΩ	
Output impedance		1.5	3.0	Ω	
Gain control range (See Fig. 5)	60	100		dB	
Maximum input (with gain reduced)		50		mVrms	10% distortion
Short circuit output current		110	200	mA	Irrespective of supply

OPERATING NOTES

Frequency Response

As with most small-signal integrated circuits, the inherent bandwidth of the SL630C is quite large. It extends from low audio frequencies up to approximately 0.5 MHz, unless restricted by a roll-off capacitor (C1) connected between pins 3 and 4. The approximate upper cut-off frequency is then given by

$$\omega_c \triangleq \frac{10^8}{C1}$$

where C1 is in picofarads

Muting

This can be achieved, in any application, by switching pin 7 directly to the negative rail

Microphone Amplifier

Fig. 2 shows the SL630C used with a balanced input on pins 5 and 6. If the load resistance increases with frequency it is necessary to stabilize the output circuitry. This is accomplished with 10Ω in series with 1nF connected between pin 1 and earth. The earth return to pin 10 must not share any common leads, particularly with the input. Decoupling pins 2 and 6 should follow normal engineering practice.

Headphone Amplifier

Fig. 3 shows the SL630C in a circuit suitable for powering a headset. The input is an unbalanced source connected to pin 5 and the device is decoupled at pins 1, 2 and 6 in the same manner as the microphone amplifier.

Manual gain adjustment using the remote gain control facility is also shown. It should be noted that the connection to pin 9 eliminates the 'dead' portion of the volume control range caused by the delayed attenuation characteristic shown in Fig. 5. R1 and R2 are chosen with regard to Fig. 5 to give the desired control range.

The input impedance at pin 8 is 3.6 kΩ.

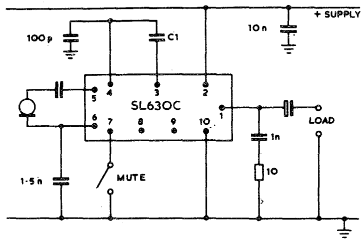


Fig 2 SL630C used as a microphone amplifier

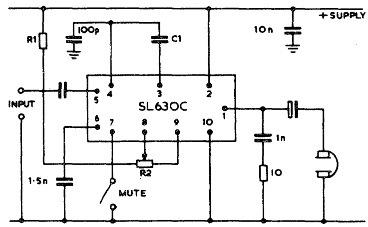


Fig 3 SL630C used as a headphone amplifier

Automatic Gain Control

To apply a.g.c., an SL620C should be used as shown in the circuit of Fig. 4. This will give effective gain control with a low audio-frequency cut-off of 200 Hz and a control response time of approximately 20 ms.

To preserve low-frequency stability and prevent motor-boating, C4 should not exceed the value given and, whilst R1 should not exceed 300Ω ,the time constant C3R1 must not be greater than 800 μs.

R2 is non-essential, but is useful if the input is likely to contain a large component below 300 Hz

C2 should be used if the power supply has a source impedance of more than a few ohms or is connected by long wires.

The system should not be tested with sinewave inputs below 300Hz as such signals can give rise to delay effects not produced by speech waveforms.

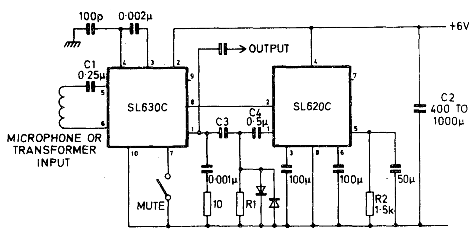


Fig 4 SL630C used with SL620C to achieve automatic gain control

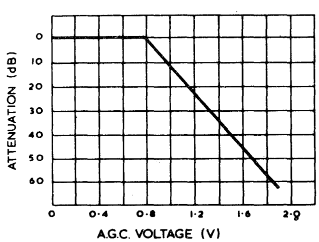


Fig 5 AGC characteristics

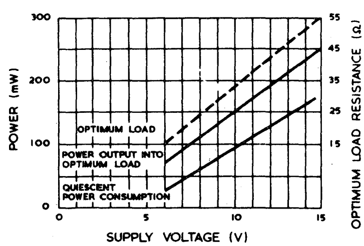


Fig 6 Power characteristics

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Free-air operating temperature range	
6V supply	−55°C to +125°C
12V supply	−55°C to +100°C
Supply voltage	+18V

SL640C & SL641C

DOUBLE BALANCED MODULATORS

The SL640C is designed to replace the conventional diode ring modulator, in RF and other communications systems, at frequencies of up to 75MHz. It offers a performance competitive with that of the diode ring while eliminating the associated transformers and heavy carrier drive power requirements.

At 30 MHz, carrier and signal leaks are typically −40dB referred to the desired output product frequency. Intermodulation products are −45dB with a 60 mV rms input signal

The SL641C is a version of the SL640C intended primarily for use in receiver mixer applications for which it offers a lower noise figure and lower power consumption. No output load resistor is included and signal leakage is higher, but otherwise the performance is identical to that of the SL640C

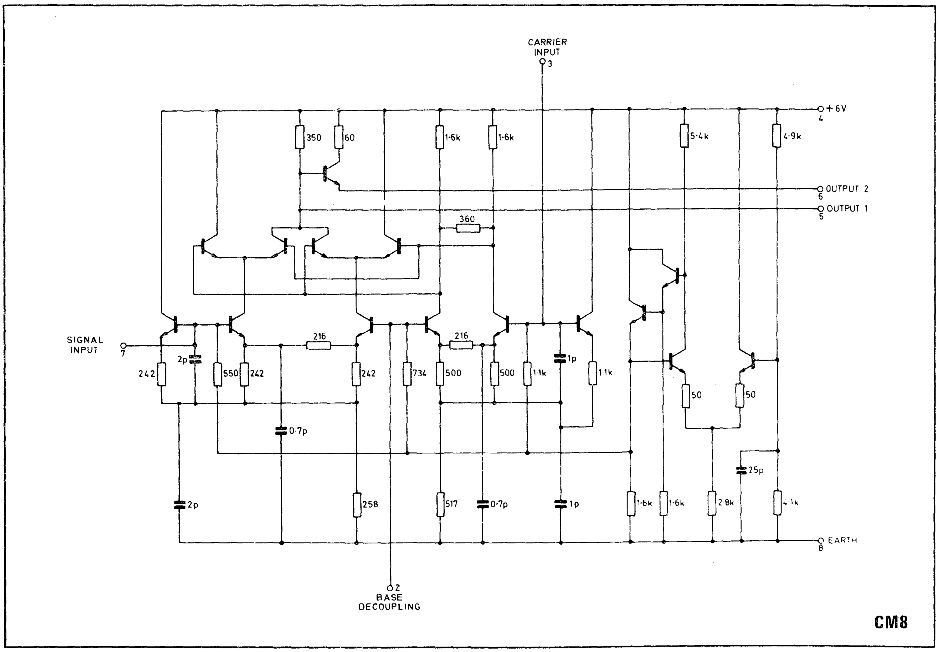


Fig. 1 Circuit diagram of SL640C

ELECTRICAL CHARACTERISTICS SL640C & SL641C

Test conditions: Supply voltage = +6V
Temperature = +25°C unless otherwise stated

Characteristic	Circuit	Value			Units	Test Conditions
		Min.	Typ.	Max.		
Conversion gain	SL640C	−2	0	+2	dB	
Signal leak $= \left[\frac{\text{Signal output}}{\text{Desired sideband output}}\right]$	SL640C		−40	−20	dB	Signal: 70mVrms, 1.75MHz Carrier: 100mVrms, 28.25MHz Output: 30MHz
Carrier leak $= \left[\frac{\text{Carrier output}}{\text{Desired sideband output}}\right]$	SL640C		−40	−20	dB	(as above)
Intermodulation products	SL640C		−45	−35	dB	Signal 1: 42.5mVrms, 1.75MHz Signal 2: 42.5mVrms, 2MHz Carrier: 100mVrms, 28.25MHz Output: 29.75MHz
Conversion transconductance	SL641C	2.2	2.5	3.5	mmho	Signal: 70mVrms, 30MHz Carrier: 100mVrms, 28.25MHz Output: 1.75MHz
Signal leak	SL641C		−18	−12	dB	(as above)
Carrier leak	SL641C		−25	−12	dB	
Intermodulation products	SL641C		−45	−30	dB	Signal 1: 42.5mVrms, 30MHz Signal 2: 42.5mVrms, 31MHz Carrier: 100mVrms, 28.25MHz Output: 3.75MHz
Carrier input impedance	Both		1kΩ & 4pF			
Signal input impedance	SL640C		500Ω & 5pF			
	SL641C		1kΩ & 4pF			
Output impedance (see Operating Notes)	SL640C		350Ω & 8pF			Output 1
	SL641C		8		pF	
Max. input before limiting	SL640C		210		mVrms	
	SL641C		250		mVrms	
Quiescent current consumption	SL640C		12	16	mA	
	SL641C		10	13	mA	
Noise figure	SL640C		15		dB	
	SL641C		12		dB	
Signal leak variation	Both		±2		dB	−55°C to +125°C
Carrier leak variation	Both		±2		dB	−55°C to +125°C
Conversion gain variation	Both		±1		dB	−55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Supply voltage	+9V
Free air operating temperature range	−55°C to +125°C

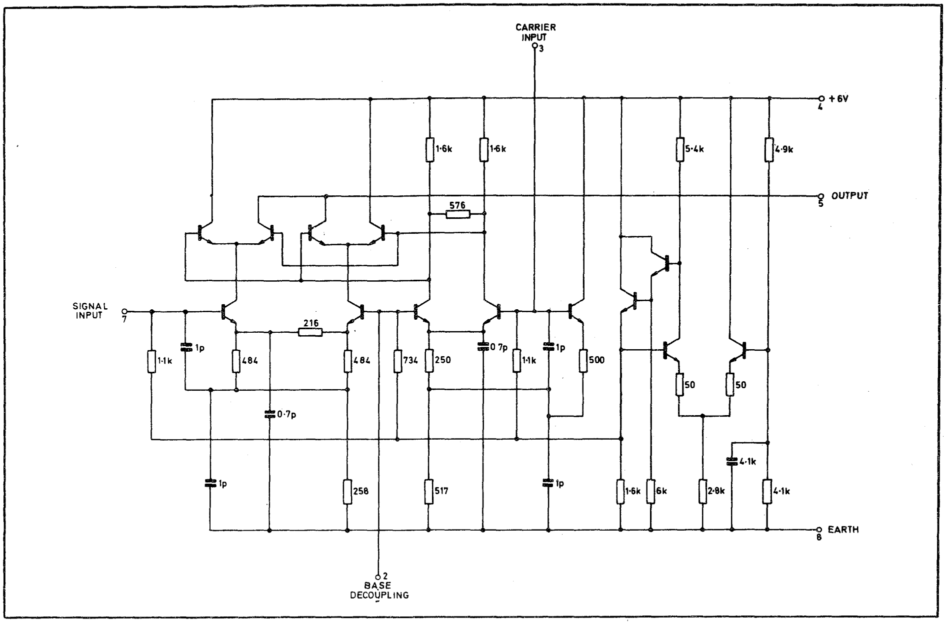


Fig. 2 Circuit diagram of SL641C

OPERATING NOTES

The SL640C circuit requires input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see electrical characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance.

Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at pin 2 would give rise to poor rejection figures and to distortion.

If the emitter follower is used, an external load resistor must be provided to supply emitter current. The quiescent output voltage from the emitter follower (pin 6) is +4.6V. To achieve maximum rejection figures at high frequencies, pin 1 (which is connected to the header) should be connected to earth and effective HT decoupling should be employed. The DC impedance should not exceed 800 ohms.

The SL641C is very similar to the SL640C but has, instead of a voltage output, a current output to enable a tuned circuit to be directly connected.

If both output sidebands are developed across the load (i.e. wideband operation), the AC impedance of the load must be less than 800Ω. If the output at one sideband frequency is negligible, the AC impedance may be raised to 1.6kΩ. It may be further raised if it is not desired to use the maximum input swing of 210mV rms.

The SL640C/641C may be used with supply voltages of up to +9 volts with increased dissipation.

Signal and carrier leaks may be minimised with 10kΩ potentiometers and 330kΩ resistors connected as shown in fig.3. R1 is adjusted to minimise signal leak; R2 to minimise carrier leak.

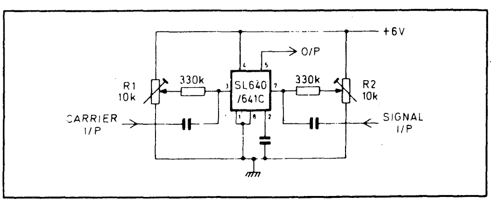


Fig. 3 Signal and carrier leak adjustments

PLESSEY
SEMICONDUCTORS

SL600 SERIES
COMMUNICATIONS CIRCUITS

SL650B & C SL651B & C
MODULATOR/PHASE LOCKED LOOP CIRCUITS

The SL650/1 are versatile integrated circuits capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using the SL650 or SL651, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage –, current –, or resistance – programmable from zero to greater than 10,000.

An auxiliary amplifier with a voltage gain of, typically, 5000 is incorpated in the SL650 for use when it is required to interface to specified levels and impedances. The auxiliary amplifier features low bias current (typically 25nA), fast recovery from overload, and a short-circuit output current of ±7.5mA.

The auxiliary amplifier is omitted from the SL651.

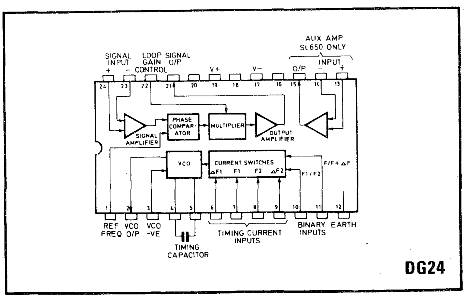


Fig. 1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100:1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient:
  'B' Types 20 ppm/°C Max.
  'C' Types 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface
- Phase Comparator O/P Can Swing to Supply Voltages
- On-Chip Auxiliary Amplifier (SL650)

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators

QUICK REFERENCE DATA

- Supply Voltages ±6V
- Operating Temperature Range –55°C to +125°C

E3▷

ELECTRICAL CHARACTERISTICS

Test Conditions

Supply voltage: ±6V
Supply currents: 1.5mA
T_A: +25°C ±5°C

Characteristics	Pins	Value Min.	Value Typ.	Value Max.	Units	Conditions
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	17, 19		±20		ppm/%	
Voltage at timing current inputs	6, 7, 8, 9		±10		mV	See note 2
VFO output, 'low' state	2		0	0.2	V	
VFO output, 'high' state	2	+1.1	+1.3		V	$R_L \geqslant 10k\Omega$
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	10, 11			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	10, 11	+2.4			V	
Input current	10, 11		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	23, 24		±2		mV	V_{out} = 0V
Input bias current	23, 24		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	23, 24		100		kΩ	
Common mode I/P voltage range	23, 24	±4			V	
Differential I/P to limit (AC)	23, 24		1.0	10	mV	See note 4
Output current	21, 22	±1.0	±2.0	±5.0	mA	I_{22} = 250μA
Current gain (pin 22 to pin 21)	21, 22	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	21,23,24	±100	±250		mA/V	See note 5
Output voltage, linear range	21	±5	±5.5		V	
Output current	21			±2	μA	I_{22} = 0
Phase comparator I/P 'low'	1	−4		−0.2	V	
Phase comparator I/P 'high'	1	+1.9		+5.3	V	
Auxiliary amplifier (SL650 only)						
Differential I/P offset voltage	13, 14		±2		mV	V_{out} = 0V
Input bias current	13, 14		0.025	0.5	μA	V_{in} = 0V
Differential I/P resistance	13, 14	0.2	3		MΩ	
Common mode I/P voltage range	13, 14	±4			V	
Voltage gain (13–14) to 15	13,14,15	1000	5000		–	
Output voltage range	15	±4	±4.8		V	$R_L \geqslant 2k\Omega$
Output current limit	15	±4	±6.5	±12	mA	

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL650C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin 21) voltage-limits first.
5. For a control current input to pin 22 of 250μA The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	± 7.5V
Storage temperature	−55° to +175°C
Operating temperature	−55° to +125°C
Input voltages	Not greater than supplies

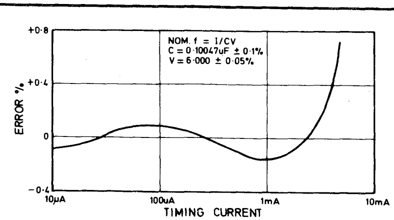


Fig.3 VFO linearity

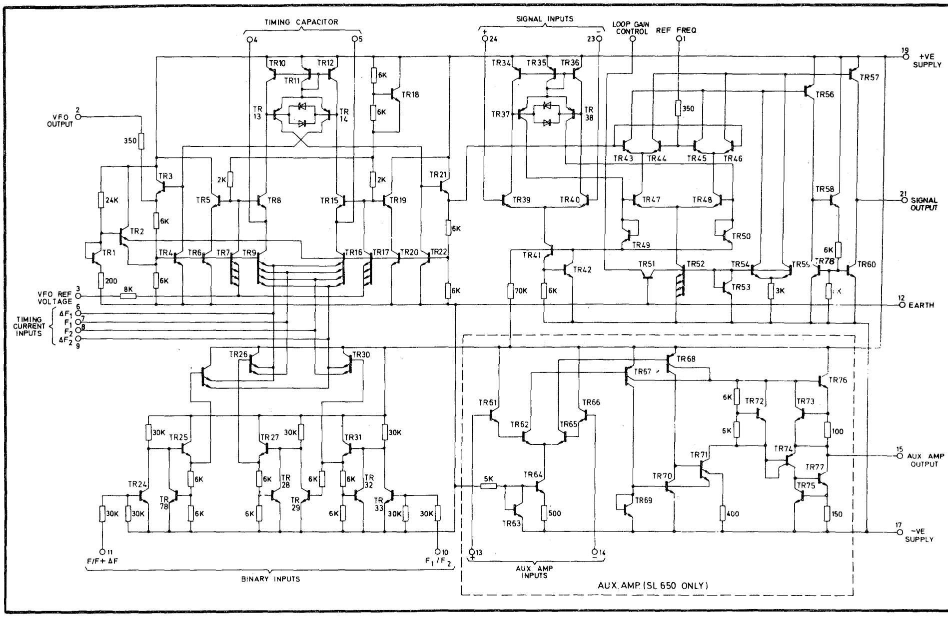


Fig. 2 Circuit diagram of SL650/SL651

OPERATING NOTES

Basic VFO Relationships

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 4 and 5, and directly proportional to the VFO timing current (see Fig.4). Four current switches, controlled by TTL-compatible logic inputs on pins 10 and 11 select a combination of external resistors (connected to pins 6, 7, 8 and 9) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to 0V however, then only the current switch associated with pin 7 is closed. The VFO timing current is then determined solely by the value of one resistor (R2 in Fig.4), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig.5, the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR} \cdot \frac{V_R}{V_3}$$

where f is in kHz, I in mA, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 3), then

$$V_R = V_3$$

$$\text{and } f = \frac{1}{CR}$$

Pin 3 is normally connected to the chip negative supply; if, however, pin 3 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR} \cdot \frac{V-}{V_C}$$

where V− is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 3

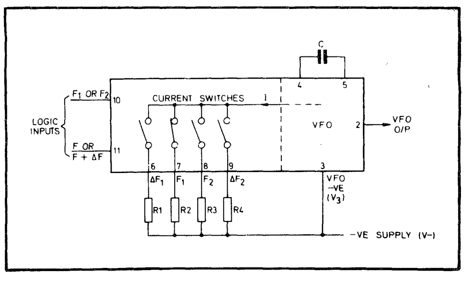


Fig.4 VFO and binary interface

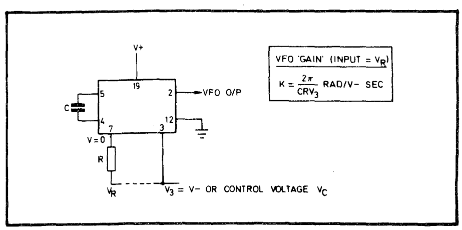


Fig.5 VFO basic configuration

The timing current I should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig.4, the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 10	Pin 11	Timing Pins	VFO Frequency
LO	LO	7	$\frac{1}{CR_2}$
LO	HI	6 & 7	$\frac{1}{CR_2} + \frac{1}{CR_1}$
HI	LO	8	$\frac{1}{CR_3}$
HI	HI	8 & 9	$\frac{1}{CR_3} + \frac{1}{CR_4}$

Table 1 Binary interface relationships

Phase Comparator

The phase comparator parameters are defined as follows (see Fig.6):

$$\text{Overall transconductance} = \frac{I_{21}}{V_{24} - V_{23}}$$

$$\text{Overall voltage gain} = \frac{V_{21}}{V_{24} - V_{23}}$$

The input amplifier will limit when the peak input $(V_{24} - V_{23})$ exceed ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

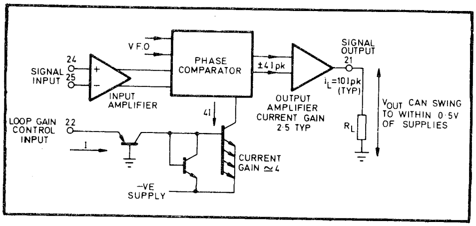


Fig.6 Phase comparator

PLESSEY SEMICONDUCTORS

TELECOMMUNICATIONS CIRCUIT

SL652C

MODULATOR/PHASE LOCKED LOOP

The SL652C is a versatile integrated circuit capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using this device, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage – current – or resistance – programmable from zero to greater than 10,000.

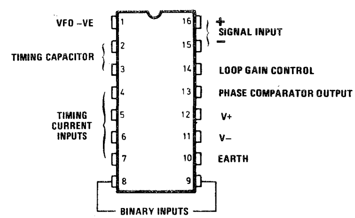


Fig. 1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100: 1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient: 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/%.Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators
- Stable Current-Controlled Oscillators

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	−55°C to +125°C
Supply Currents	1.5mA typ.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±7.5V
Storage temperature	−55° to +175°C
Operating temperature	−55° to +125°C
Input voltages	Not greater than supplies

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltage: ±6V
T_A: +25°C ±5°C

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	11, 12		±20		ppm/%	
Voltage at timing current inputs	4, 5, 6, 7		±10		mV	See note 2
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	8, 9			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	8, 9	+2.4			V	
Input current	8, 9		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	15, 16		±2		mV	V_{out} = 0V
Input bias current	15, 16		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	15, 16		100		kΩ	
Common mode I/P voltage range	15, 16	± 4			V	
Differential I/P to limit (AC)	15, 16		1.0	10	mV	See note 4
Output current	13, 14	±1.0	±2.0	±5.0	mA	I_{14} = 250μA
Current gain (pin 14 to pin 13)	13, 14	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	13, 15, 16	±100	±250		mA/V	See note 5
Output voltage, linear range	13	±5	±5.5		V	
Output current	13			±2	μA	I_{14} = 0

NOTES
1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL652C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin. 13) voltage-limits first.
5. For a control current input to pin. 14 of 250μA. The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

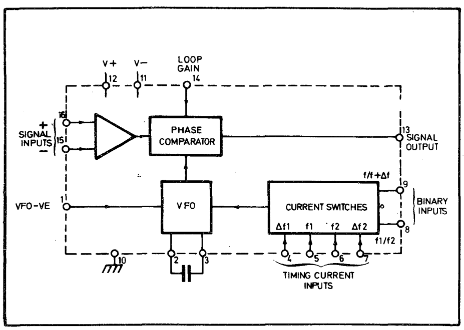


Fig. 2 SL652C block diagram

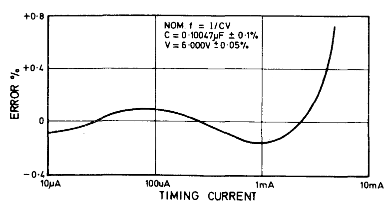


Fig. 3 VFO linearity

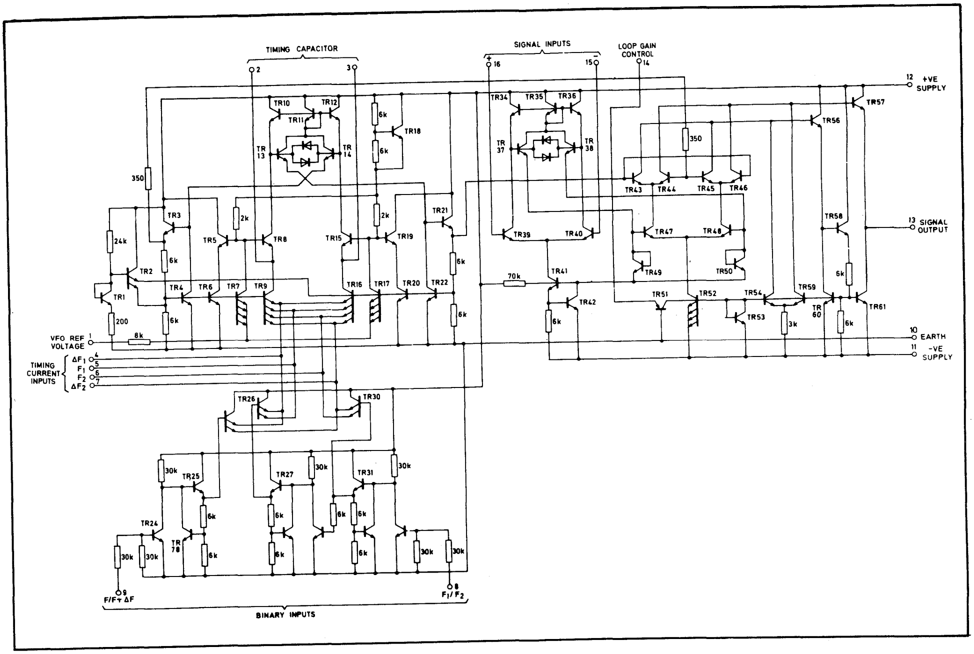


Fig. 4 Circuit diagram of SL652

OPERATING NOTES

Basic VFO Relationships

The oscillator output is normally taken from the phase comparator output by biasing the signal inputs a few hundred millivolts apart. If a direct oscillator output is required when the phase comparator is otherwise employed, it should be taken from pin 2 or 3 (which may affect oscillator stability). Alternatively, an SL651C can be used in place of the SL652C.

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 2 and 3, and directly proportional to the VFO timing current (see Fig. 5). Four current switches, controlled by TTL-compatible logic inputs on pins 8 and 9 select a combination of external resistors (connected to pins 4, 5, 6 and 7) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to OV however, then only the current switch associated with pin 5 is closed. The VFO timing current is then determined solely by the value of one resistor (R2 in Fig. 5), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig. 6 the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR}\frac{V_R}{V_1}$$

where f is in kHz, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 1) then

$$V_R = V_1$$

$$\text{and } f = \frac{1}{CR}$$

Pin 1 is normally connected to the chip negative supply; if, however, pin 1 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR}\frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 1.

The timing current should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig. 5, the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 8	Pin 9	Timing Pins	VFO Frequency
LO	LO	5	$\frac{1}{CR_2}$
LO	HI	4 & 5	$\frac{1}{CR_2}+\frac{1}{CR_1}$
HI	LO	6	$\frac{1}{CR_3}$
HI	HI	6 & 7	$\frac{1}{CR_3}+\frac{1}{CR_4}$

Table 1 Binary interface relationships

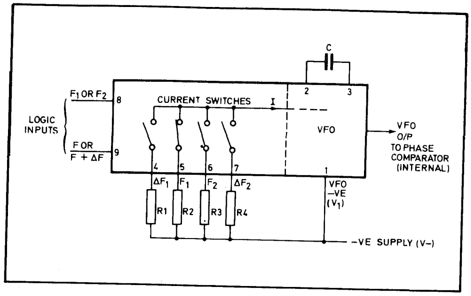


Fig. 5 VFO and binary interface

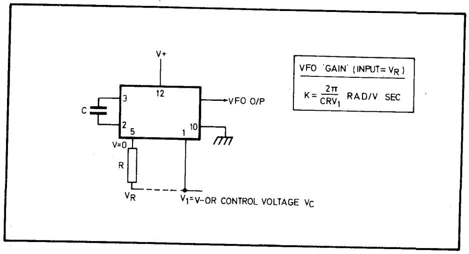


Fig. 6 VFO basic configuration

Phase Comparator

The phase comparator parameters are defined as follows (see Fig. 7):

$$\text{Overall transconductance} = \frac{I_{13}}{V_{16} - V_{15}}$$

$$\text{Overall voltage gain} = \frac{V_{13}}{V_{16} - V_{15}}$$

The input amplifier will limit when the peak input ($V_{16} - V_{15}$) exceeds ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

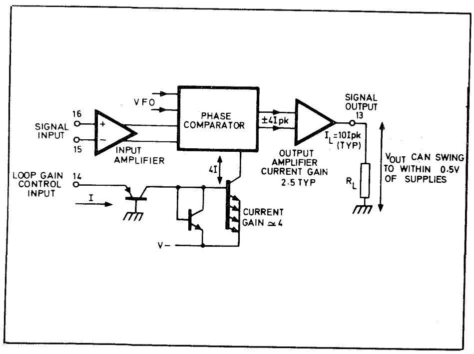


Fig. 7 Phase comparator

PLESSEY
SEMICONDUCTORS

SL500 SERIES
WIDEBAND AMPLIFIERS

SL561C
ULTRA LOW NOISE PREAMPLIFIERS

This integrated circuit is a high gain, low noise preamplifier designed for use in audio and video systems at frequencies up to 6MHz. Operation at low frequencies is eased by the small size of the external components and the low 1/*f* noise. Noise performance is optimised for source impedances between 20Ω and 1kΩ making the device suitable for use with a number of transducers including photo-conductive IR detectors, magnetic tape heads and dynamic microphones.

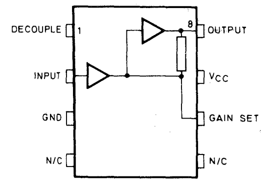


Fig. 1 Pin connections (viewed from the top)

APPLICATIONS

- Audio Preamplifiers (low noise from low impedance source)
- Video Preamplifier
- Preamplifier for use in Low Cost Infra-Red Systems

FEATURES

- High Gain 60dB
- Low noise 0.8nV/√Hz (Rs = 50Ω)
- Bandwidth 6MHz
- Low Power Consumption 10mW (V_{CC} = 5V)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Vcc 5V
Source impedance 50Ω
Load impedance 10kΩ
T_{amb} 25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	57	60	63	dB	Pin 6 0/C
Equivalent input noise voltage		0.8		nV√Hz	100Hz to 6MHz
Input resistance		3		kΩ	
Input capacitance		15		pF	
Output impedance		50		Ω	
Output voltage	2	3		V p-p	See note 4
Supply current		2	3	mA	
Bandwidth		6		MHz	

OPERATING NOTES

1. Upper cut-off frequency
The bandwidth of the amplifier can be reduced from 6MHz to any desired value by a capacitor from pin 6 to ground. This is shown in Fig. 5. No degradation in noise or output swing occurs when this capacitor is used. The high frequency roll off is approximately 6dB/ octave.

2. Low frequency reponse
The capacitors C_2 and C_3 (Fig. 4) determine the lower cut-off frequency. C_2 decouples an internal feedback loop and if its value is close to that of C_3 an increase in gain at low frequencies can occur. For a flat response make $0.05\,C_3 > C_2 > 5C_3$.

3. Gain set facility
Provision is made to adjust the gain by means of a resistor between pin 6 and the output. Gains as low as 10dB can be selected. This resistor increases the feedback around the output stage and stability problems can result if the bandwidth of the amplifier is not reduced as indicated in Note 1. Fig.6 shows recommended values of C_1 for each gain range. Since the input stage is a common emitter stage without emitter degeneration (for best noise) at values of gain less than 40dB this input stage, rather than the output stage, determines the maximum output voltage swing. For a distortion of less than 10% the input voltage should be restricted to less than 5mV.

4. Driving low impedance loads
The quiescent current of the output emitter follower is 0.5mA. If larger voltage swings are required into low impedance loads this current can be increased by a resistor from pin 8 to ground. To avoid exceeding the ratings of the output transistor the resistor should not be less than 200Ω.

5. Noise performance
The equivalent input voltage for the amplifier is shown in Fig.7. From this the input noise voltage and current generators can be derived. They are :-

$$e_n = 0.8\text{nV}/\sqrt{\text{Hz}}$$
$$i_n = 2.0\text{pA}/\sqrt{\text{Hz}}$$

Flicker or 1/f noise is not normally a problem, the knee frequency being typically below 100Hz.

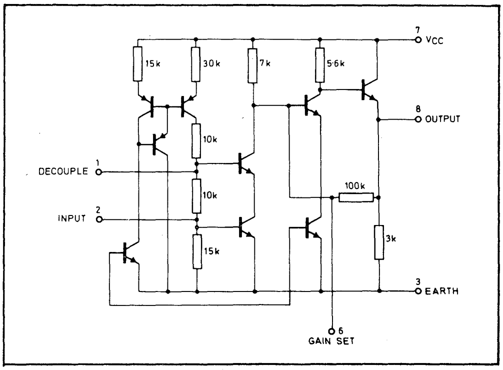


Fig. 2 Circuit diagram

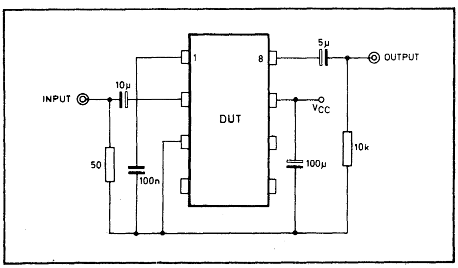


Fig. 3 Test circuit

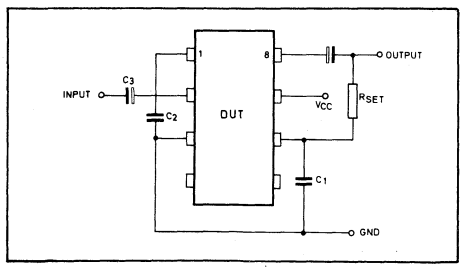


Fig. 4 Typical application

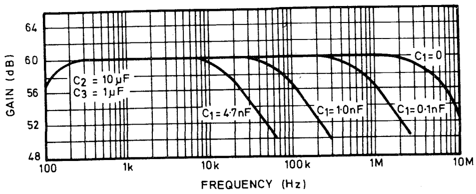


Fig. 5 Gain v. frequency

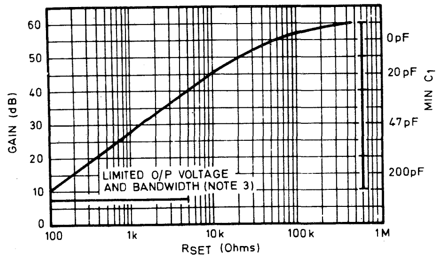


Fig. 6 Gain v. R_{set}

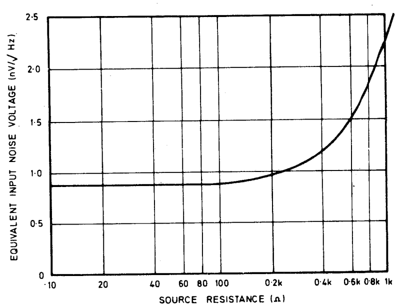


Fig. 7 Noise v. source impedance

PLESSEY
SEMICONDUCTORS

SL600 SERIES
COMMUNICATIONS CIRCUITS

SL664C / SL665C

LOW POWER IF/AF CIRCUITS FOR NARROW BAND FM

The SL664 and SL665 independently perform the IF/AF function of a low power FM receiver. Each circuit is a complete IF strip and consists of a pre-amplifier, limiting amplifier, quadrature detector, carrier squelch, DC volume control and audio output stage. The SL664 and SL665 differ in that the SL664 features a power audio output stage (typically 250mW into 8Ω) whilst the SL665 has a low level audio output which drives high impedance loads (open collector output). With the SL664 the demodulator and audio amplifier are muted by the squelch output. The SL665 squelch output does not internally mute the demodulator, which means that it can be used for tone decoding. If, on the SL665, the squelch function is not required then, with some additional circuitry, (see Fig. 6) a signal strength meter can be incorporated.

APPLICATIONS

- Mobile Radio
- Hand Held Radio

FEATURES

- Low Power
- Purpose Designed for Narrow Band
- Carrier Squelch

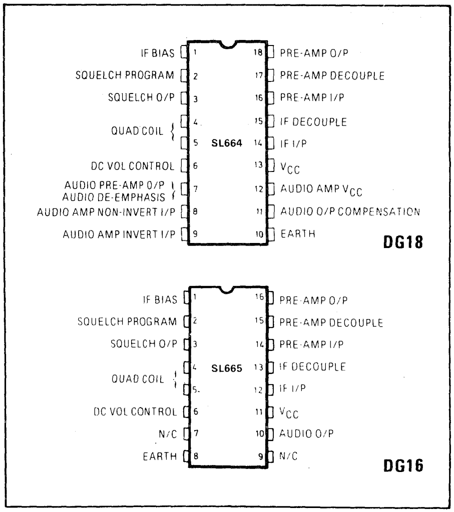


Fig. 1 Pin connections

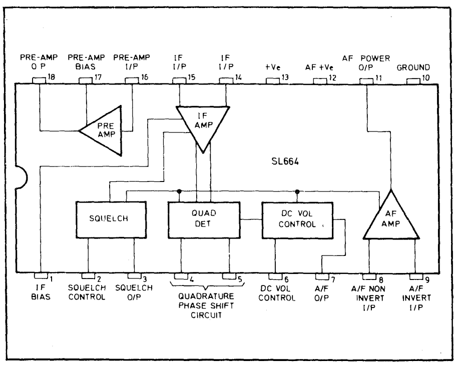


Fig. 2 SL664 logic diagram

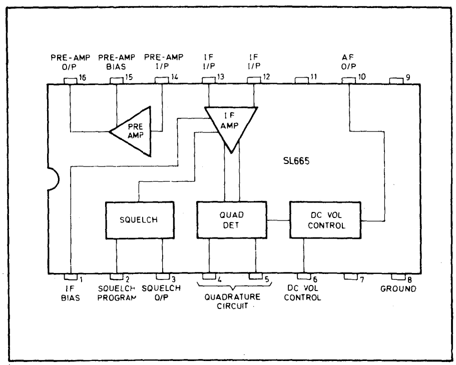


Fig. 3 SL665 logic diagram

ELECTRICAL CHARACTERISTICS—SL664

Test conditions (unless otherwise stated):
Supply voltage, V_{cc} = 6V
Ambient temperature, T_A = 22°C ± 2°C
IF = 10.7 MHz, Deviation = 5kHz (peak),
Modulating frequency = 1kHz

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply voltage	4.5	6	12	V	
Supply current		3,5	6.0	mA	Muted
Supply current		10	13	mA	Unmuted
Pre-amp gain		46		dB	
Limiter gain		60		dB	
Combined 3dB bandwidth		25		MHz	
S/N ratio		50		dB	1mVrms input
Sensitivity	10			µV	20dB S/N
AM rejection		35		dB	1mVrms input30% AM
Audio O/P power		250		mW	R_L = 8Ω
Distortion, THD			3	%	5%THD, 150mW O/P
Squelch range		45		dB	
Squelch law		2		µA/dB	
Squelch hysteresis		10		dB	Hysteresis resistor = 360kΩ
DC volume control range	50	70		dB	
DC volume control law		2		µA/dB	
Squelch O/P low level		1	1.5	V	100µVrms input
Squelch O/P high level	4.5	5		V	No input

ELECTRICAL CHARACTERISTICS—SL665

As above except:

Characteristics	Min.	Typ.	Max.	Units	Conditions
Supply current		6	9.5	mA	
Audio O/P level		25		mV RMS	1mVrms input, RL = 10 kΩ

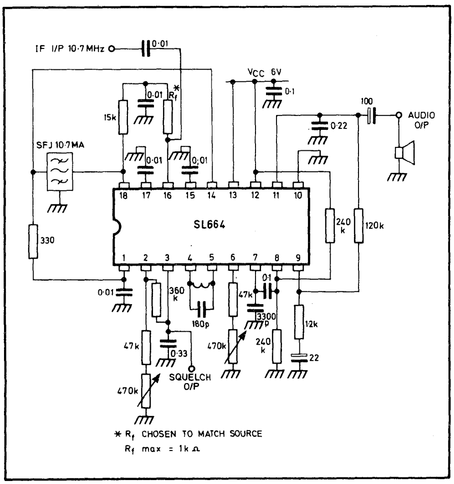


Fig. 4 SL664 test circuit

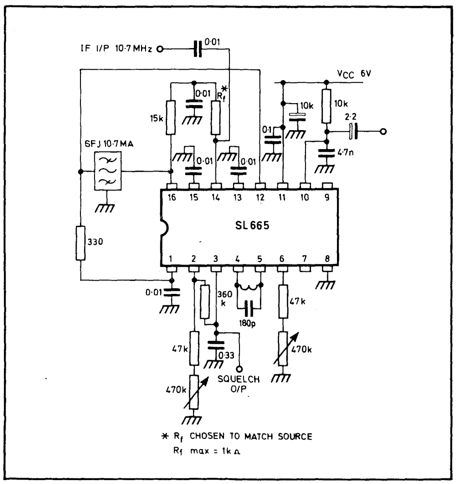


Fig. 5 SL665 test circuit

APPLICATION NOTE

The detector characteristics depend upon the quadrature circuitry used. The SL664 and SL665 have been designed to permit the use of high-Q quadrature circuits.

A quadrature circuit using a 'Q' of approximately 140 can be made with an air cored coil of 25 turns 30 SWG cotton covered wire on a neosid A7 former tuned by a 150pF ceramic capacitor in parallel with a 30pF trimmer.

SFJ 10.7MA filters made by Murata (Distributed by Pedoka, London).

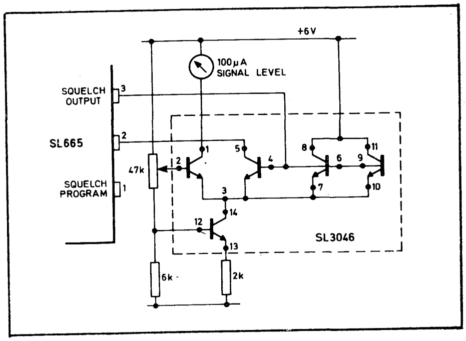


Fig. 6 Signal level meter application

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	—55°C to +150°C
Operating temperature range	—30°C to +85°C
Supply voltage	+14V

PLESSEY
SEMICONDUCTORS

SL680C SL1680C

CRYSTAL OSCILLATOR MAINTAINING CIRCUITS

The SL680C and SL1680C are bipolar integrated circuits designed to maintain the oscillation of an external series resonant crystal without significant degradation of frequency stability. The sinewave output has about 3% harmonic distortion and its level is independant of crystal activity. Crystals may be used in their fundamental or overtone modes with only minor circuit changes.

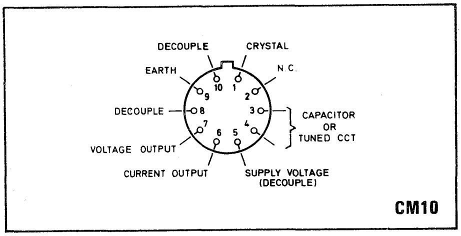


Fig. 1 Pin connections, SL680C

FEATURES

- Insignificant Degradation of Crystal Frequency Stability.
- Frequency Range 100 kHz to 100 MHz.
- Output Level Independent of Crystal Parameters.
- Overtone Crystals Can Be Used.
- Voltage and Current Outputs Provided.
- Harmonic Distortion Typically Less Than 3%.
- Very Low Crystal Power

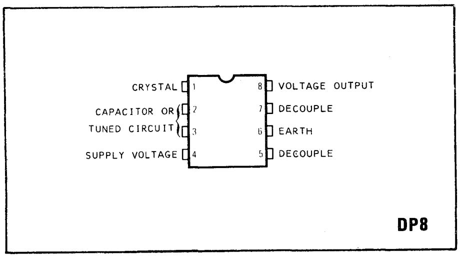


Fig. 2 Pin connections, SL1680C

OPERATING NOTES

A block diagram of the SL680C/1680C is shown in Fig. 3. The circuit consists of a single transistor amplifier with the crystal decoupling its emitter. The output of this amplifier drives a fixed gain amplifier with an emitter follower output capable of voltage driving low impedance loads, and a free collector output for driving fixed impedances or tuned circuits (SL680C only).

The output from the fixed gain amplifier also goes to a detector and, via a variable attenuator, to the base of the single transistor amplifier. The variable attenuator is controlled by the detector output. The circuit contains an internal supply regulator, enabling it to be operated from a range of supply voltages.

In operation, the signal fed back to the tuned single transistor amplifier causes the system to oscillate at the resonant frequency of the crystal. A DC signal derived from the output level of the fixed gain amplifier and applied to the attenuator maintains the output at constant level irrespective of the activity of the crystal.

The phase shift through the system has been kept as low as possible and, even more importantly, varies very little with temperature or power supply voltage. Since varying phase shift is the commonest cause of varying frequency in crystal oscillators (with the exception, of course, of variations in the crystals themselves) this low phase shift ensures that the oscillator's frequency variation with temperature and supply voltage will be minimal. The actual values will depend upon the crystal used but typical temperature variation is 10—3 ppm/ °C over the

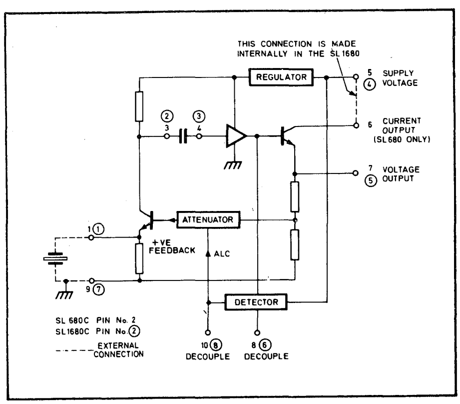


Fig. 3 SL680C/1680C block diagram

range —10 °C to +80 °C and 10^{-1} ppm/V over a power supply range of 6 to 10 volts. These figures are independent of any variations due to the crystal itself.

Variations in the crystal are often caused by excessive power dissipation. The SL680C/SL1680C is unlikely to suffer from this problem since the crystal dissipation is held to the order of 0.5µ Watt.

Coupling between the tuned amplifier and the fixed gain amplifier is usually by a capacitor and the circuit oscillates at the crystal's fundamental frequency. If overtone operation is required the coupling must be by a high pass filter to ensure that the loop gain at the overtone exceeds the loop gain at the fundamental. For third Overtone operation this high pass filter may be as simple as a very small value capacitor but for higher overtones a tuned circuit of some sort is necessary.

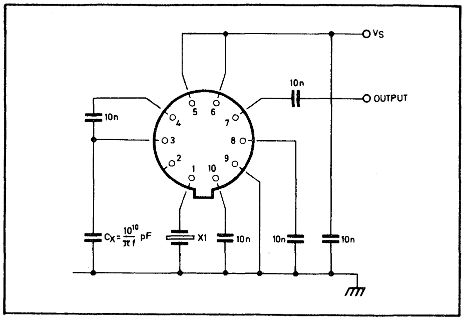
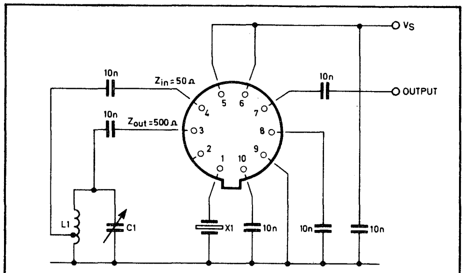


Fig. 4 Fundamental test circuit



1. LICI tuned to required overtone.
2. CRYSTAL X1 = CATHODEON TYPE BO 7211

Fig. 5 Third overtone test circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

Temperature	22 °C ± 2 °C
Supply Voltage	6V
Load Impedance	500Ω
Crystal Fundamental 16.3 MHz (series mode)	

Characteristic	Value Min.	Typ.	Max.	Units	Conditions
Output Voltage	0.1	0.15	0.2	Vrms	SL680C
	0.08	0.15	0.22	Vrms	SL1680C
Supply Current		7	15	mA	SL680C
		7			SL1680C
Max. operating frequency		100		MHz	
Current output		1		mAp—p	SL680C
Harmonic output		—30		dB	wrt 16.3MHz output
Frequency error (note 1)		5		ppm	
Frequency stability (note 2)		0.1		ppm/volt	Vs=6V to 10V
		10^{-3}		ppm/°C	—10 °C to +80 °C
Crystal dissipation		50Rs		nW	Rs = Crystal series loss resistance

NOTES
1. The frequency error is the difference between frequency of oscillation obtained using the SL680C/SL1680C and the frequency obtained in a zero phase measurement system such as described in BS9610.
2. These stability figures are dependant on the crystal used and are given for guidance only.

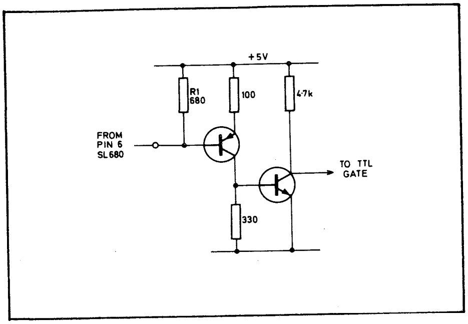


Fig. 6 Buffer for driving TTL

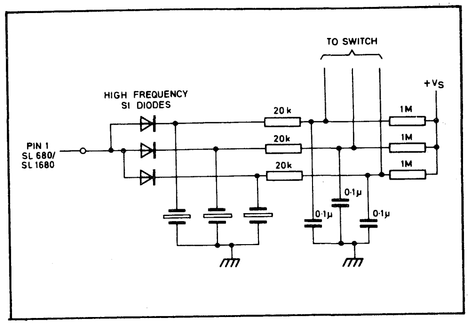


Fig. 7 Crystal selection interface

Absolute Maximum Ratings

(Non-simultaneous)

Storage temperature: SL680C —55°C to +150°C
SL1680C —30°C to +85°C
Operating temperature: SL680C —55°C to +125°C
SL1680C —30°C to +70°C
Supply voltage +12V

PLESSEY
SEMICONDUCTORS

SL700 SERIES
OPERATIONAL AMPLIFIERS

SL701B&C SL702B&C SL751B&C

The SL701B, SL701C, SL702B, SL702C, SL751B and SL751C are monolithic, bipolar integrated circuit, high gain D-C amplifiers, intended primarily for use as operational amplifiers or in instrumentation applications. The SL701 basic circuit has an internal zener and provides an output symmetrical about earth when using the specified supply voltage. The SL702 basic circuit is non-symmetrical, with a direct output, but may be used with an external zener to permit a symmetrical output to be obtained at other supply voltages. The SL751 basic circuit has both the internal zener and a direct output and may be used in either application.

The SL701C, SL702C and SL751C differ from their equivalent devices with suffix B mainly in having higher maximum input offset voltage.

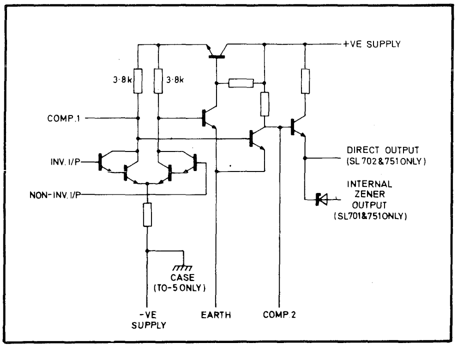


Fig. 2 Circuit diagram

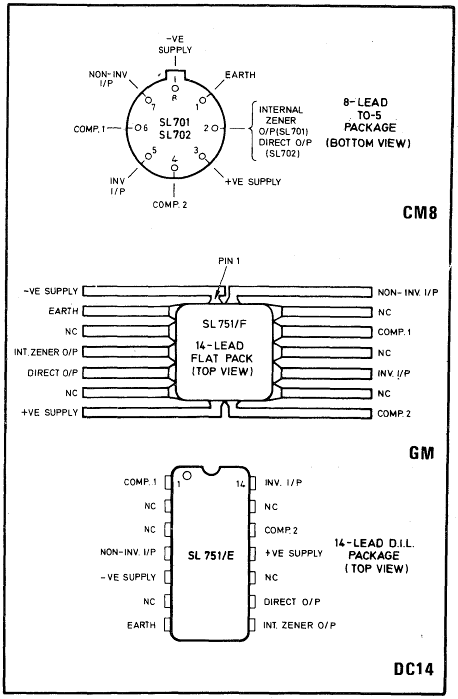


Fig. 1 Pin connections

ELECTRICAL CHARACTERISTICS

Test Conditions: (unless otherwise stated)

T_{amb} = +22°C ± 2°C

Supplies = +12V and −12V

A 6.0V zener is added to SL702 except where otherwise stated. (See test circuits)

Characteristic	Circuit	Value			Units	Test conditions	Test Fig. 3
		Min.	Typ.	Max.			
Open loop gain (Fig. 5)	All	66	70	78	dB	Frequency = 30kHz	A
Change of gain with temperature	All		±2		dB	Frequency = 20kHz −25°C to +100°C	A

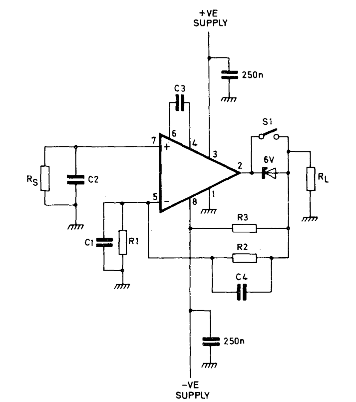
Characteristic	Circuit	Value			Units	Test Conditions	Test Fig. 3
		Min.	Typ.	Max.			
Open loop andwidth (Fig. 5)	All	250	500		kHz	High frequency −3dB point	A
Output resistance	All		100		Ω	1kHz	A
Input resistance	All		100		kΩ	1kHz	A
180° phase shift frequency (Fig. 5)	All	20	35		MHz		A
Input offset voltage	SL701B, SL702B and SL751B			5	mV		1
Input offset voltage	SL701C, SL702C and SL751C			20	mV		1
Input offset voltage change with temperature	All		15		μV/°O		1
Input current	SL701B, SL702B and SL751B			1	μA		G & H
Input current	SL701C, SL702C and SL751C			3	μA		G & H
Input offset current	SL701B, SL702B and SL751B			0.3	μA		F
Input offset current	SL701C, SL702C and SL751C			1.8	μA		F
Input offset current change with temperature (see Note)	All		0.4		μA	−25°C to +100°C	F
Common mode rejection ratio (Fig. 4)	SL701B, SL702B and SL751B	70	80		dB	+0.5V to −3V input square wave	
Common mode rejection ratio (Fig. 4)	SL701C, SL702C and SL751C	60	80		dB	+0.5V to −3V input square wave	
Supply line rejection	All	60	70		dB	1.0V square wave on supply line	
Positive output clipping level (DC)	All	+3.9	+4.3		V		C
Negative output clipping level (DC)	All	−6.0	−6.5		V		C
Positive output clipping level (DC)	SL702B & C SL751B & C (direct O/P)	+ 9.9	+10.3		V	No external zener	C(S1 closed)
Negative output clipping level (DC)	SL702B & C SL751B & C (direct O/P)	0	−0.5		V	No external zener	C(S1 closed)
Positive supply line current	All	9.5	12	14.5	mA	Output at 0V (R3 ± 2% tolerance)	A
Negative supply line current	All	7.5	9	10.5	mA	Output at Ov (R3 ± 2% tolerance)	A
Spot noise	All		See Fig. 7			Open loop	

NOTE

Total change in offset current over specified range

Test reference	$R_S(\Omega)$	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	R_L	*C_1 (μF)	C_2 (nF)	C_3	C_4 (pF)	Remarks
A (Fig. 5 & 10)	50	o/c	100	2.2	o/c	30	o/c	o/c	o/c	Open loop AC gain (Figs. 5 and 10)
B (Fig. 5)	50	o/c	100	2.2	o/c	30	o/c	33pF	o/c	Compensated open loop AC gain (Fig. 5)
C (Fig. 6 & 10)	50	1	99	2.2	o/c	o/c	o/c	33pF	o/c	Gain of 100 (Figs 6 and 10)
D (Fig. 6 & 10)	50	1	9	2.2	o/c	o/c	o/c	33pF	4.7	Gain of 10 (Figs. 6 and 10)
E (Fig. 8)	50	1	99	Varied	Varied	30	o/c	o/c	o/c	Negative swing/load resistance (Fig. 8)
F	100k	o/c	100	2.2	o/c	4	1	1nF	o/c	Input offset current
G	100k	o/c	s/c	2.2	o/c	4	1	1nF	o/c	Input current
H	s/c	o/c	100	2.2	o/c	4	o/c	1nF	o/c	Input current
I	s/c	o/c	s/c	2.2	o/c	4	o/c	1nF	o/c	Input offset voltage

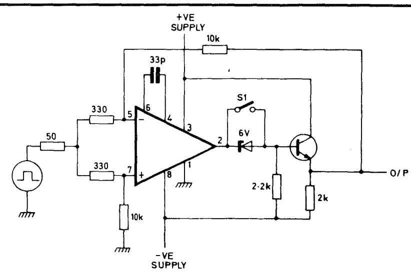
*C_1 should be a non-polarized tantalum or paper type.



NOTES

1. AMPLIFIER PIN CONNECTIONS SHOWN APPLY TO SL701 (S1 CLOSED) AND SL702 (S1 OPEN EXCEPT WHERE OTHERWISE STATED). FOR SL751 CONNECTIONS SEE FIG. 1.

Fig. 3 Test circuit



NOTES

1. THE 330Ω RESISTORS ARE MATCHED TO 0.02% AND THE 10kΩ RESISTORS ARE MATCHED TO 0.05%.
2. AMPLIFIER PIN CONNECTIONS SHOWN APPLY TO SL701 (S1 CLOSED) AND SL702 (S1 OPEN). FOR SL751 CONNECTIONS SEE FIG. 1.

Fig. 4 Common mode test circuit

The test circuit of Fig. 3 is used for measuring all electrical characteristics except common mode rejection. Component values for tests A to I using Fig. 3 are given in the following table.

Frequency Response and Feedback Stabilization

The typical gain/phase frequency response of the device is given in Fig. 5. When the external feedback connections are made the resultant loop gain must be cut at a mean rate of less than 9–10 db/octave. A single dominant time constant is often the simplest solution. For example, in the SL701 and similar amplifiers, a capacitor between pins 5

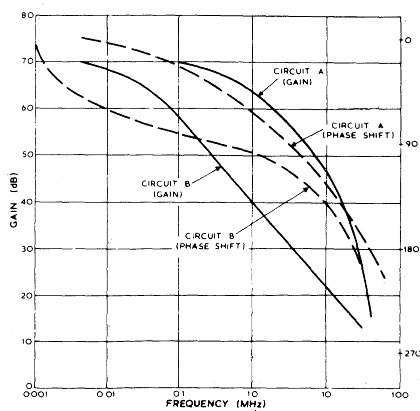


Fig. 5 Open loop gain and phase shift v frequency

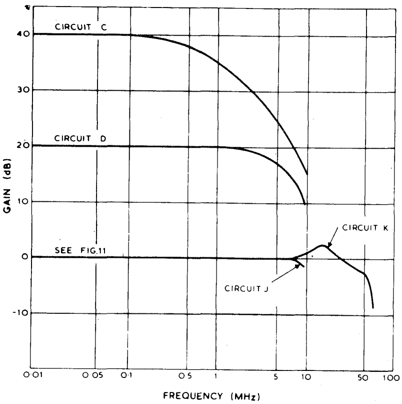


Fig. 6 *Gain with feedback v frequency*

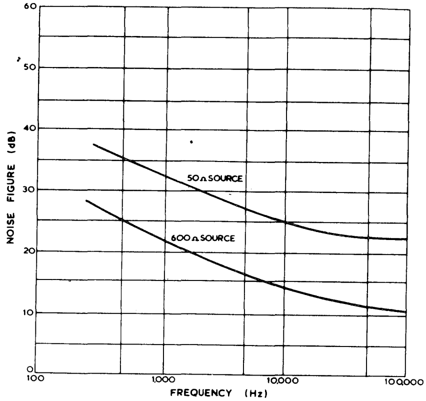


Fig. 7 *Spot noise v frequency (open loop)*

and 7 with a value between a few tens and a few hundred pF (depending on the feedback fraction) will give a suitable dominant high frequency cut-off. In general, however, when a particular feedback loop is designed, an appropriate stabilizing arrangement, to suit it, will be needed. Except when maximum bandwidth is required, a dominant lag provided by a 33 pF stabilizing capacitor will be found satisfactory for loop gains up to about 20 dB short of the full forward gain of the amplifier; gain curves for this configuration are given in Fig. 6.

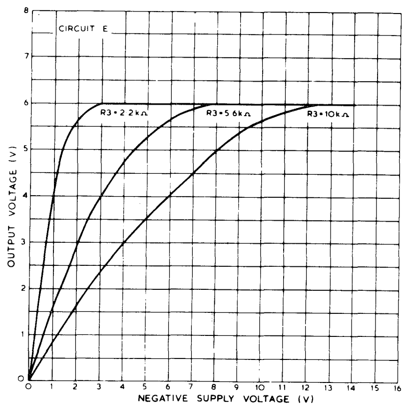


Fig. 8 *Max. negative swing as a function of load resistance*

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Supply voltage (Fig. 11)	+ 14V and −14V
Output current	20mA
Input voltage (either input, opposite input at 0V)	+1V to − 10V.

Amplifier dissipation at different supply voltages

The curves assume zero load current is drawn from the output. Assuming that a resistor R_3 (zener bias resistor — Fig. 8) is connected between the output and the negative line, the total maximum dissipation will be obtained by adding the power term:

$$\frac{|-V|.|+V|}{R_3}$$

to the value obtained from Fig. 11.

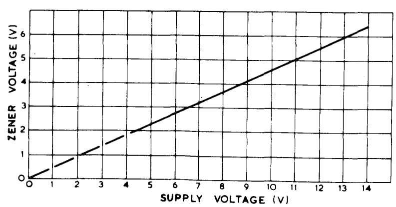


Fig. 9 *Zener voltage v supply voltage for symmetrical output about earth*

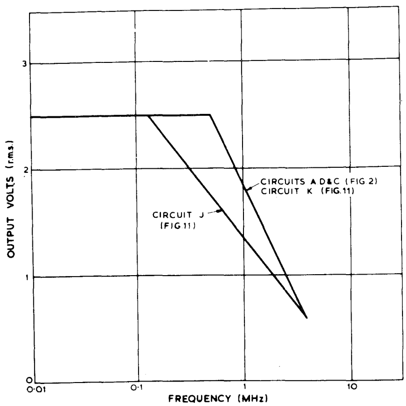


Fig. 10 Typical max. output v frequency

OPERATING NOTES

Lower Supply Voltages (SL702 and SL751 – with direct output)

The balance of the collector currents of the input transistors is maintained by an auxiliary internal feedback loop, enabling a range of supply voltages to be used, as shown in Fig. 9 and Fig. 11. Since the collector currents of the input transistor are controlled by a 3k Ω 'tail' resistor, the input base current and offset current will decrease and the input resistance will increase as the negative supply rail voltage is reduced. The open loop gain is also affected by this rail voltage and is virtually proportional to it. A reduction in the positive rail voltage does little except decrease various currents and voltages within the circuit; together with the negative supply this decreases the maximum available output level. In order to avoid internal limiting, the magnitude of the positive supply must not be very much lower than that of the negative supply; hence at levels less than the nominal ± 12 volts, attention must be paid to the tolerance of the supplies. Typical characteristics for operation under these conditions are given below.

Test conditions: Supply voltages +6V and –6V
Ambient temperature = +20°C
External zener = 2.7V
Test circuits as above

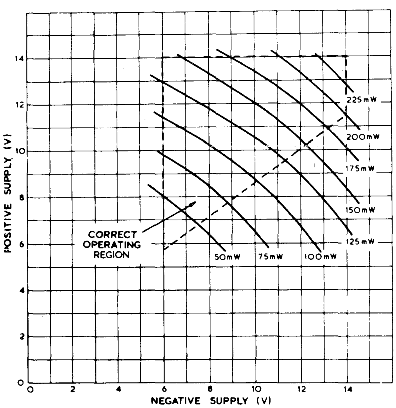


Fig. 11 Amplifier dissipation at different supply voltages

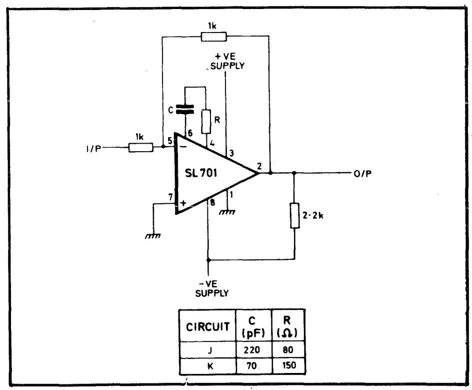


Fig. 12 Unity gain test circuit (tests J and K)

Characteristic	Value	Units	Test conditions
Open loop gain	62	dB	
Input resistance	200	kΩ	
Max. input base current (SL702B, SL751B) (see note)	500	nA	
Max. input base current (SL702C, SL751C) (see note)	1.5	μA	
Max. input offset current (SL702B, SL751B) (see note)	150	nA	
Max. input offset current (SL702C, SL751C) (see note)	900	nA	
Supply current (+ve)	8	mA	R_3 = 1.2k Ω ± 2%
Supply current (–ve)	6.5	mA	R_3 = 1.2k Ω ± 2%
Output clipping level (+ve)	2	V	
Output clipping level (–ve)	3	V	

NOTE

These figures are not guaranteed, but indicate relation to full specification at ± 12V supplies.

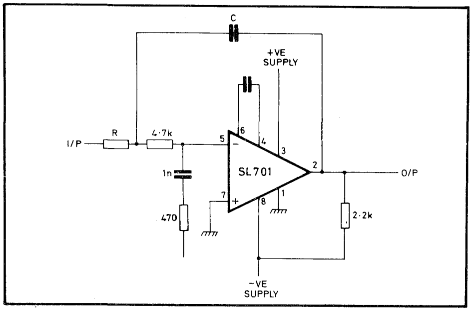


Fig. 13 Integrator circuit

Unity Gain

For unity gain more than one method of compensation may be employed; the simplest is shown in Fig. 12. The disadvantages of the method suggested are that some peculiar overload characteristics may be observed at high frequencies and the maximum signal output without limiting is lower than at higher circuit gains. Circuit K on Fig. 12 gives compensation for wideband response, allowing approximately 1 dB gain rise above the gain at low frequencies. For maximum signal handling, but reduced noise performance, the method as indicated in Fig. 13 may be used.

DEFINITION OF TERMS

Decibel (dB) Units Refers to the conventional expression of a voltage ratio in logarithmic units, i.e. $20 \log_{10} V_2/V_1$ dB.

Open Loop Bandwidth The frequency at which the open loop gain falls by 3 dB (factor $\sqrt{2}$) below the value at 1kHz.

Output Resistance The ratio of change in output voltage to the change in output current, measured at the output terminal, under open loop conditions and with zero volts d.c. output level.

Input Resistance The resistance between the input terminals, equivalent at low frequencies to the resistance between input and earth with the other input earthed.

180° Phase Shift Frequency The lowest frequency at which the output phase is shifted 180°, relative to the low frequency value, compared to the input signal under open loop conditions with no compensation capacitors.

Input Offset Voltage The voltage between the input terminals to set the DC output voltage to zero.

Input Current The base current of either input transistor when the DC output voltage is set to zero.

Input Offset Current The difference between the input currents when the output quiescent voltage is zero.

Common mode rejection The ratio between the common mode signal and a differential signal producing the same magnitude of output (dB units).

Supply Line Rejection The ratio between the supply line signal and a differential input producing the same magnitude of output (dB units).

Output Clipping Levels The DC voltage at the output terminal when a voltage of ± 0.1V is applied between the input terminals (Gain x 100, circuit C).

PLESSEY
SEMICONDUCTORS

SL700 SERIES
OPERATIONAL AMPLIFIERS

SL748A&C
PRECISION OPERATIONAL AMPLIFIER

The SL748 is a monolithic Precision Operational Amplifier. It is an excellent choice when performance versus cost trade-offs are possible between super beta or FET input operational amplifier and low cost general purpose operational amplifiers. The low offset and bias currents of the SL748 improve system accuracy in applications such as long term integrators, sample and hold circuits and high source impedance summing amplifiers. Even though the input bias current is extremely low, the SL748 maintains full ±30V differential voltage range. The internal construction utilizes isothermal layout and special electrical design to maintain system performance despite variations in temperature or output load. High common mode input voltage range, latch-up protection, short circuit protection and simple frequency compensation make the device versatile and easy to use.

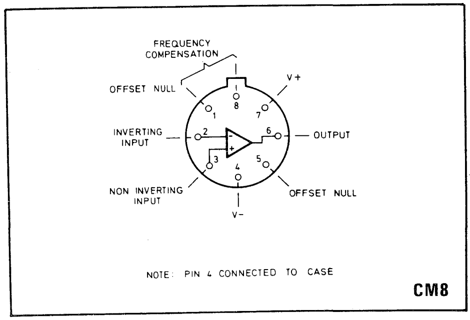


Fig. 1 Pin connections

FEATURES

- Low Offset Voltage and Offset Current
- Low Offset Voltage and Current Drift
- Low Input Bias Current
- Low Input Noise Voltage
- Large Common-mode and Differential Voltage Ranges

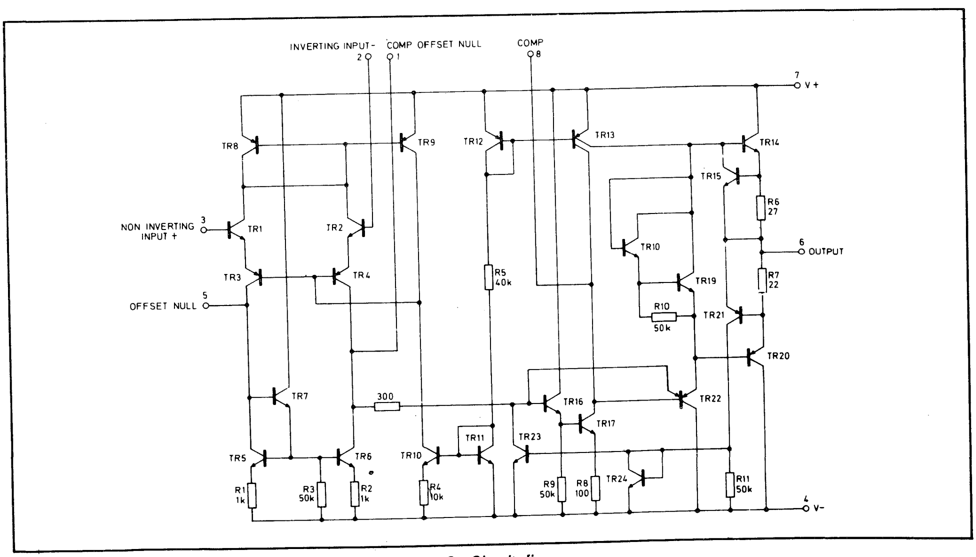


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS (SL748A)

Test conditions (unless otherwise stated)
V_S = ±15V
T_A = +25°C
C_C = 30pF

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Condition
Input offset voltage		1.0	5.0	mV	$R_S \leqslant 10k\Omega$
Input offset current		20	200	nA	
Input bias current		80	500	nA	
Input resistance	0.3	2.0		MΩ	
Input capacitance		2.0		pF	
Offset voltage adjustment range		±15		mV	
Large signal voltage gain	50000	200000		V/V	$R_L \geqslant 2k\Omega$ V_{OUT} = ±10V
Output resistance		75		Ω	
Output short-circuit current		25		mA	
Supply current		1.9	2.8	mA	
Power consumption		60	85	mW	
Transient response (voltage follower, gain of 1)					V_{IN} = 20mV, C_C = 30pF, R_L = 2kΩ, $C_L \leqslant$ 100pF
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew rate (voltage follower, gain of 1)		0.5		V/μs	$R_L \geqslant 2k\Omega$, C_C = 30pF
Transient response (voltage follower, gain of 10)					V_{IN} = 20mV, C_C = 3.5pF, R_L = 2kΩ, $C_L \leqslant$ 100pF
Risetime		0.2		μs	
Overshoot		5.0		%	
Slew rate (voltage follower, gain of 10)		5.5		V/μs	$R_L \geqslant 2k\Omega$, C_C = 3.5pF
The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$					
Input offset voltage		1.0	6.0	mV	$R_S \leqslant 10k\Omega$
Input offset current		10	200	nA	T_A = +125°C
		50	500	nA	T_A = −55°C
Input bias current		0.03	0.5	μA	T_A = +125°C
		0.3	1.5	μA	T_A = −55°C
Input voltage range	±12	±13		V	
Common mode rejection ratio	70	90		dB	$R_S \leqslant 10k\Omega$
Supply voltage rejection ratio		30	150	μV/V	$R_S \leqslant 10k\Omega$
Large signal voltage gain	25000			V/V	$R_L \geqslant 2k\Omega$, V_{OUT} = ±10V
Output voltage swing	±12	±14		V	$R_L \geqslant 10k\Omega$
	±10	±13		V	$R_L \geqslant 2k\Omega$
Supply current		1.5	2.5	mA	T_A = +125°C
		2.0	3.3	mA	T_A = −55°C
Power consumption		45	75	mW	T_A = +125°C
		60	100	mW	T_A = −55°C

ELECTRICAL CHARACTERISTICS (SL748C)

Test conditions (unless otherwise stated)

$V_S = \pm 15V$
$T_A = +25°C$
$C_C = 30pF$

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Input offset voltage		2.0	6.0	mV	$R_S \leqslant 10k\Omega$
Input offset current		20	200	nA	
Input bias current		80	500	nA	
Input resistance	0.3	2.0		MΩ	
Input capacitance		2.0		pF	
Offset voltage adjustment range		±15		mV	
Large signal voltage gain	20000	150000		V/V	$R_L \geqslant 2k\Omega$, $V_{OUT} = \pm 10V$
Output resistance		75		Ω	
Output short-circuit current		25		mA	
Supply current		1.9	2.8	mA	
Power consumption		60	85	mW	
Transient response (voltage follower, gain of 1)					$V_{IN} = 20mV$, $C_C = 30pF$, $R_L = 2k\Omega$ $C_L \leqslant 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew rate (voltage follower, gain of 1)		0.5		V/μs	$R_L \geqslant 2k\Omega$, $C_C = 30pF$
Transient response (voltage follower, gain of 10)					$V_{IN} = 20mV$, $C_C = 3.5pF$, $R_L = 2k\Omega$, $C_L \leqslant 100pF$
Risetime		0.2		μs	
Overshoot		5.0		%	
Slew rate (voltage follower, gain of 10)		5.5		V/μs	$R_L \geqslant 2k\Omega$, $C_C = 3.5pF$
The following specifications apply for $0°C \leqslant T_A \leqslant +70°C$					
Input offset voltage			7.5	mV	$R_S \leqslant 10k\Omega$
Input offset current			300	nA	
Input bias current			800	nA	
Input voltage range	±12	±13		V	
Common mode rejection ratio	70	90		dB	$R_S \leqslant 10k\Omega$
Supply voltage rejection ratio		30	150	μV/V	$R_S \leqslant 10k\Omega$
Large signal voltage gain	15000			V/V	$R_L \geqslant 2k\Omega$, $V_{OUT} = \pm 10V$
Output voltage swing	±12	±14		V	$R_L \geqslant 10k\Omega$
	±10	±13		V	$R_L \geqslant 2k\Omega$
Power consumption		60	100	mW	

ABSOLUTE MAXIMUM RATINGS

Supply voltage	±22V (SL748A) ±18V (SL748C)
Internal power dissipation	500mW
Differential input voltage	±30V
Input voltage	±15V
Storage temperature range	−65°C to +150°C
Operating temperature range	
Military (SL748A)	−55°C to +125°C
Commercial (SL748C)	0°C to 70°C
Lead temperature (soldering 60 seconds)	300°C
Output short-circuit duration	Indefinite

PLESSEY
SEMICONDUCTORS

SL1000 SERIES
TELECOMMUNICATIONS CIRCUITS

SL1001A & B
MODULATOR/DEMODULATOR

The SL1001A and B are bipolar monolithic integrated circuit double balanced modulators, designed primarily for use in telephone transmission equipment, but equally suitable for any application where the modulation function is required.

The devices employ conventional 'tree' configuration multiplier circuits. Careful design of the circuit layout results in low carrier and signal leak levels, with high dynamic range and good linearity. Internal bias is provided, allowing direct balanced transformer input, or single-ended capacitor drive.

A two-stage common collector output structure is used to provide a low output impedance.

A pair of diodes is included to provide optional carrier input limiting.

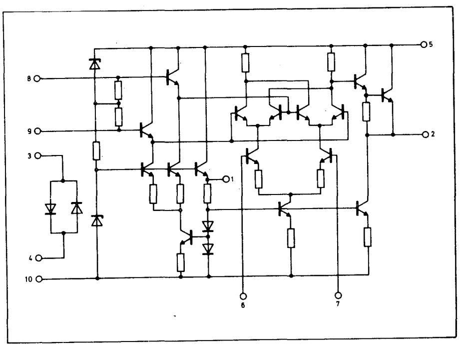


Fig.1 Circuit diagram

FEATURES

- High Carrier and Signal Suppression: 50dB
- Unity Conversion Gain
- Low Noise Level: −112dBmp
- High Intermodulation Suppression: 58dB
- Low Supply Current: 4mA
- Diodes included for Limiting

APPLICATIONS

- Telephone Transmission Equipment
- Suppressed Carrier and Amplitude Modulation
- Synchronous Detection
- FM Detection
- Phase Detection

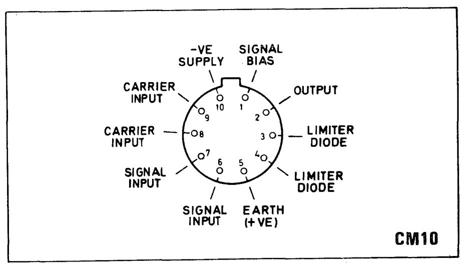


Fig.2 Pin connections (bottom)

QUICK REFERENCE DATA

Supply Voltage	−15V
Supply Current SL1001A	6mA
Supply Current SL1001B	4mA
Carrier Level	125mVrms (MIN.)
Signal Level	Up to 600mVrms
Output Current SL1001A	3.5mA peak (TYP.)
Output Current SL1001B	2.0mA peak (TYP.)
Temperature Range	−25°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 22°C ± 2°C
Circuit ref: Figs.3 and 4

Characteristic	Value Min.	Value Typ.	Value Max	Units	Conditions
Conversion gain	− 1	0	+1	dB	
Signal input impedance		150		kΩ	Pins 6 & 7
Carrier input impedance	7	10	13	kΩ	Pins 8 & 9
	3.3	5	6.7	kΩ	Pins 8 & 5 or 9 & 5
Output impedance					
SL1001A		12		Ω	Pin 2
SL1001B		25		Ω	Pin 2
Signal suppression	20	50		dB	Signal 170mV, Carrier 500mV
Carrier suppression	20	40		dB	Signal 170mV, Carrier 500mV
2nd harmonic suppression		40		dB	Signal 170mV, Carrier 500mV
Carrier compression			0.1	dB	For ± 3dB on 500mV
Supply line suppression	50			dB	Line impedance 500Ω
Sig. and carrier band width	200			kHz	
Carrier level	125			mVrms	
Signal level			600	mVrms	
Output current					
SL1001A		3.5		mApk	
SL1001B		2.0		mApk	
Noise level		− 112	− 105	dBmp	Weighted speech band
Intermod. products		− 58		dB	Signals 2 X 170mV
Gain stability		0.12		dB	+5°C to +55°C
		0		dB	± 10% supply
Adjusted carrier suppression		70		dB	See Fig.5

ABSOLUTE MAXIMUM RATINGS

Supply voltage (via 820Ω)	−30V
Storage temp. range	−55°C to + 175°C
Free air operating temp. range	−40°C to + 150°C

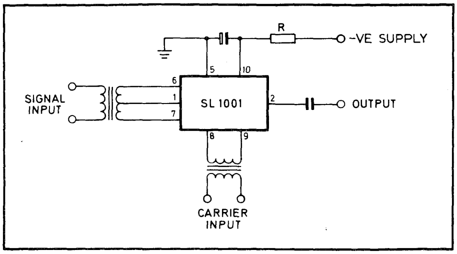


Fig.3 Transformer input

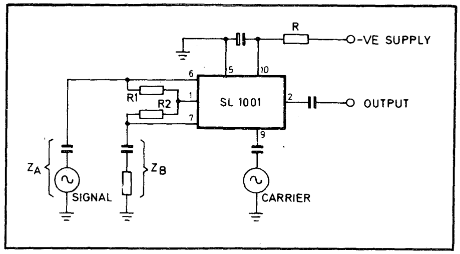


Fig.4 Unbalanced input

OPERATING CONDITIONS (see Figs.3 and 4)

Parameter	Value	Units	Condition
Supply voltage	−15	V	Pin 10
Supply current			
SL1001A	6	mA	
SL1001B	4	mA	
Input bias current	5	μA	Pins 6 & 7
Dynamic resistance	8	kΩ	Pins 5 to 10
Output quiescent voltage	−3	V	Pins 2 to 5
Temperature range	−25 to +125	°C	

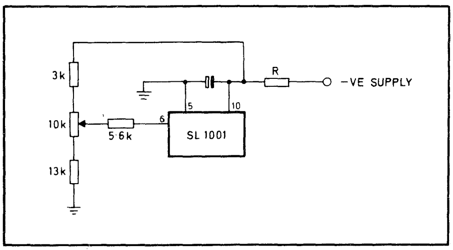


Fig.5 Carrier suppression adjustment

OPERATING NOTES

1. A resistance in series with the supply (Pin 10) is usually advisable, to improve the supply rejection and reduce the circuit voltage.
2. For good carrier suppression, the signal input bias resistors should be equal and have a value less than 5kΩ
3. For improved intermodulation suppression, Pin 1 may be decoupled, preferably with a 100Ω resistor in series with Pin 1.

   If Pin 1 is not decoupled, noise is optimised when an unbalanced drive is used, by providing equal source impedances for Pins 6 and 7.
4. Low leakage input capacitors are advisable for the input connections to avoid inducing carrier or signal leakage.
5. Carrier suppression may be improved by using the circuit of Fig.5, and adjusting for minimum leakage.

PLESSEY
SEMICONDUCTORS

SL1000 SERIES
TELECOMMUNICATIONS CIRCUITS

SL1021 A & B
CHANNEL AMPLIFIER

The SL1021 A and B are bipolar monolithic integrated circuit amplifiers designed for use as channel amplifiers in telephone transmission equipment and satisfy the requirements of the British Post Office channel translating apparatus (RC5467).

The two variants A and B are distinguished by guaranteed output levels of +10dBm and +13dBm, respectively, other parameters being identical.

The main feature of these devices is the provision of a temperature-stable DC operated remote gain control facility having an adjustable range of control.

The connections provided allow a variety of uses, including fixed gain amplification with various feedback configurations.

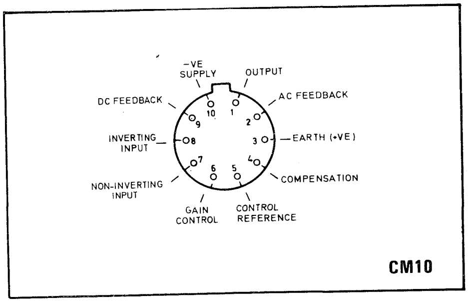


Fig. 1 Pin connections

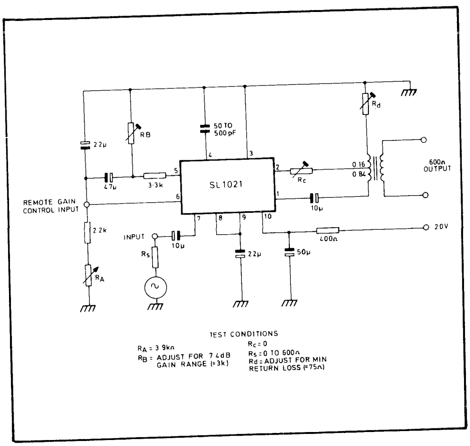


Fig. 2 SL1021 test circuit and typical application

FEATURES

- Up to +13dBm O/P into 600Ω (Class A)
- Temperature insensitive remote DC gain control
- Non-interactive adjustment of:
  - Gain
  - Gain Range
  - Output Return Loss
- 1:1 600Ω Transformer output can be optimized for low inductance using 2-element filter configuration
- Power Bandwidth: 150kHz (fixed gain, Fig. 4)
- Small Signal - gain Bandwidth: 3MHz (see Fig. 4)

QUICK REFERENCE DATA

Supply Voltage	−20V (via 400Ω)
Supply Current	9mA
Gain Control Current	0.5mA
Temperature Range	−25°C to +125°C

APPLICATIONS

- Telephone Communications
- Channel Group Translation Equipment
- Radio – communications
- Small Signal Processing

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} 22°C ± 2°C

These characteristics are those obtained using the test circuit of Fig.1, the gain range and output impedance being adjusted as indicated.

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
Gain (reference gain G)	24.5	26	27.5	dB	
Gain/R_S			28	dB	R_S = 600Ω to 3kΩ
Gain range		7.4		dB	Adjusted
Gain law					
R_A = 125Ω	3.9	4.1	4.3	dB	Relative to G
R_A = 9kΩ	−3.5	−3.3	−3.1	dB	
Gain/temperature	−0.1		+0.1	dB	Relative to G, T = 10°C to 45°C
Gain/V_S			0.1	dB	V_S = −20V ± 1V
Distortion					
2nd harmonic			−36	dBm0	At 10dBm output
3rd harmonic			−45	dBm0	
Overload					
SL1021A	10	13		dBm	Class A operation
SL1021B	13	15		dBm	
Noise			−76	dBmP	Proportional to G
Output impedance		600		Ω	Adjusted
Return loss	20			dB	250Hz to 3.4kHz
Input impedance	10			kΩ	Variable with R_A and R_S
Gain at reduced V_S	25.5			dB	V_S = −17.5V See Fig.1
Overload at reduced V_S	7			dBm	V_S = −17.5V
Gain control interaction between channels (change in gain for 3.3 mA current change)			0.25	dB	Equivalent to 11 channels, Common R_A earth return
Frequency response	240		3400	Hz	±0.05dB ref. 800Hz
Bandwidth			100	kHz	C_C = 50pF

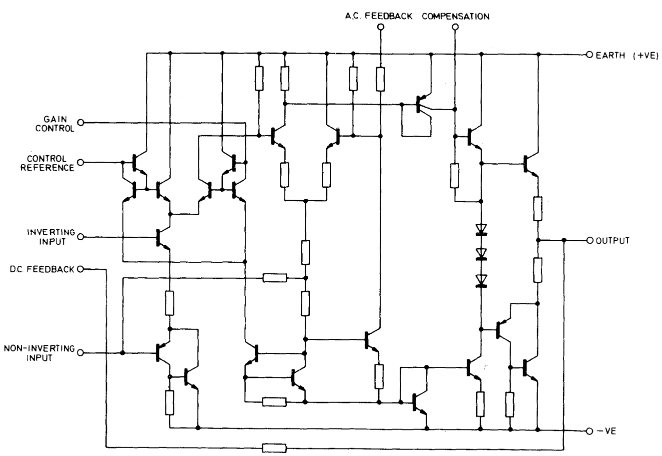


Fig. 3 SL1021 equivalent circuit

OPERATING CONDITIONS (See Fig. 1)

Parameter	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply current		9	11.0	mA	$R_A = 0$
		7.0		mA	$R_A = 11k\Omega$
Supply voltage		–20		V	Via 400Ω
Supply voltage on chip		–17		V	Pin 10
Supply maximum			–23	V	Pin 10
Control current		0.5		mA	$R_A = 0$
		0.26		mA	$R_A = 10k\Omega$
Control current change			0.3	mA	$R_A = 0$ to $11k\Omega$
Operational temp.	–25		+125	°C	
Fixed gain application (see Fig. 4)					
Optimum load		100		Ω	
Power output		20		mW	Class AB
Power bandwidth		150		kHz	10mW
Gain		20		dB	Values as Fig. 4
Frequency response		3		MHz	Small signal

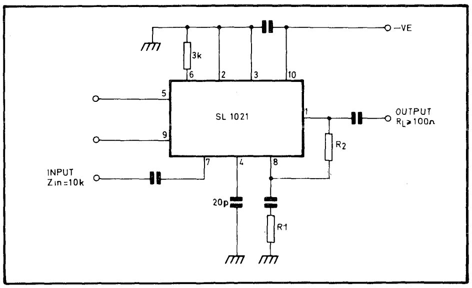


Fig. 4 Fixed gain amplifier, Class A or AB

OPERATING NOTES

1. The control decoupling capacitors should be of a low leakage type.
2. Other values of control resistors are possible if other gains/gain ranges are required. However, the parallel resistance to earth from pins 5 and 6 should be ⩽8kΩ at all settings.
3. If the control resistance is increased or open circuited, the amplifier gain will decrease to zero. (See Fig. 4 for fixed gain use).
4. The compensation capacitor C_c can be increased to reduce the frequency response at the expense of the power bandwidth.
5. The gain may be increased from the value of Fig. 1 (26dB nominal) by increasing R_c, the gain increase being given by:

$$\frac{R_c + 8.5}{8.5} \pm 20\%$$

where R_c is in kΩ.

Because of temperature coefficient mismatch between R_C and internal resistors, the gain stability may be degraded with temperature.

6. The case is connected to pin 10 (–ve supply). To avoid damage to the device when operating with a positive earth system, care should be taken to prevent the case from becoming earthed.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (via 400Ω)	–30V
Storage temp. range	–55°C to +175°C
Free air operating temp. range	–40°C to +130°C

SL1025B
BALANCED MODULATOR

The SL1025B is a bipolar integrated circuit intended for use as a double balanced modulator. Although primarily designed for FDM telephone transmission equipment as a channel modulator/demodulator, it is equally suitable for use as an analogue multiplier.

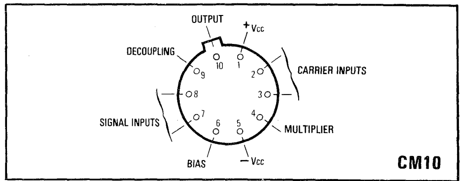


Fig. 1 Pin connections (bottom)

FEATURES

- High Carrier and Signal Suppression: 50dB typ.
- High Conversion Gain: 5dB typ.
- Low Supply Current: 2.5mA max.
- Can be used as an Analogue Multiplier.

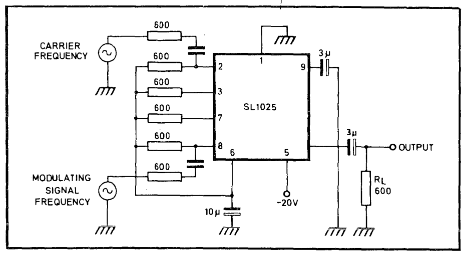


Fig. 2 Modulator using single supply voltage

APPLICATIONS

- Telephone Transmission Equipment
- Suppressed Carrier and Amplitude Modulation
- Synchronous Detection
- AC and DC Multipliers
- Automatic Gain Control
- Frequency Doublers

QUICK REFERENCE DATA

- Supply Voltage 20V
- Operating Temperature Range —20°C to +85°C
- Supply Current 2mA typ

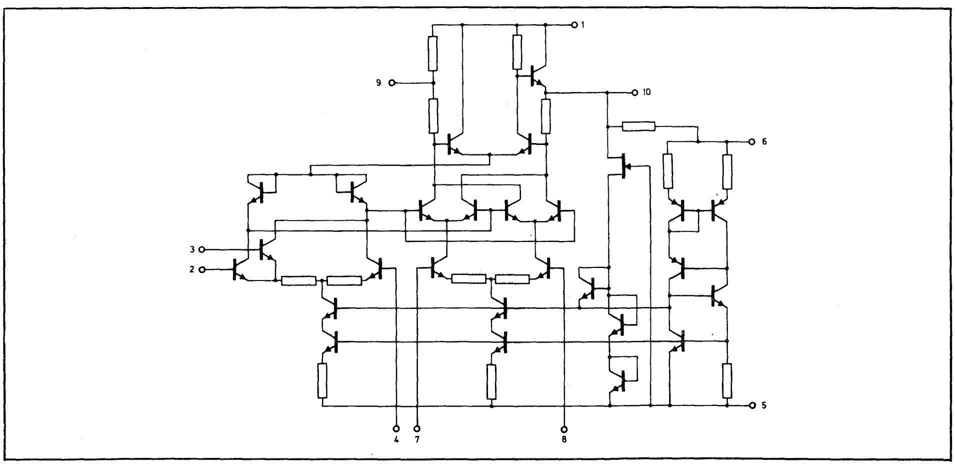


Fig. 3 Circuit diagram of SL1025

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltages: ±10V
T_A: +25°C
Carrier frequency: 130kHz
Signal frequency: 25kHz
Circuit ref.: Fig. 2.

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Total supply voltage operating range	12		30	V	Pin 1 (pos), pin 5 (neg.)
Supply current		2	2.5	mA	Vcc= ±10V
Input bias current			2	µA	Inputs 2, 3
			2	µA	Inputs 2, 4
			4	µA	Inputs 7, 8
Quiescent output voltage	+5.4	+6.2	+6.8	V	Pin 10, no signal or carrier inputs
Differential output voltage		25	100	mV	Pins 9, 10
Reference voltage		+2.5		V	Pin 6
Input impedance		30		kΩ	Input 2, 3
		300		kΩ	Inputs 2, 4
		150		kΩ	Inputs 7, 8
Output voltage swing	1	1.3		Vp-p	Pin 10
Output impedance		3	10	Ω	Pin 10
Conversion gain	4.5	5.0	5.5	dB	Output 140mV, carrier 150mV
Signal suppression	35	50		dB	Signal 200mV, 25kHz
Carrier suppression	35	50		dB	Carrier 200mV, 130kHz
Second harmonic suppression		75		dB	Signal, carrier 200mV
Intermodulation products		−60		dB	Signal, carrier 200mV

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30V
Differential input voltage	±5V
Power dissipation (70°C)	300mW
Storage temperature	−55°C to 150°C
Operating temperature	−20°C to +85°C

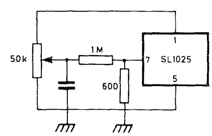


Fig. 4 Adjusting carrier leakage of SL1025

APPLICATIONS

Modulator

The basic circuit of a double sideband, suppressed carrier, double balanced modulator is shown in Fig. 2. When separate positive and negative supplies are used pin 6 is left open circuit; the input coupling capacitors are no longer required and inputs are referred to 0V.

To ensure the modulated output has an amplitude dependent only on the signal input the carrier is internally amplitude limited. A carrier input of approximately 150mV RMS is normally sufficient to allow this.

Conversion gain is substantially independent of temperature, supply voltage and frequency up to 1MHz. Carrier leakage increases substantially over 1MHz and it becomes necessary to provide some form of nulling adjustment. A suitable circuit is shown in Fig. 4.

Output levels are chosen as a compromise between distortion at high levels and leakage or noise at low levels. Outputs in the region of 150mV RMS are normally used. If the circuit is required to drive low impedance loads (300 ohms and below) it is advisable to connect a 15k resistor externally between pins 5 and 10.

Multiplier

To use the SL1025 as a multiplier then inputs 2 and 4 become 'X' inputs; 7 and 8 are the 'Y' inputs. The Y channel has slightly lower offset voltage and lower distortion but the performance is still sufficient to build a four quadrant DC multiplier with less than 1% overall distortion.

The Scale Factor (approximately 3.2) is virtually independent of supply voltage, temperature and frequency up to 1MHz. Typical transfer characteristics are shown in Fig. 5.

To obtain complementary outputs for driving an operational amplifier it is permissable to use pin 9 in addition to the normal output, pin 10. It is generally necessary to add external resistors between pin 9 and the voltage supplies to improve linearity and voltage swing.

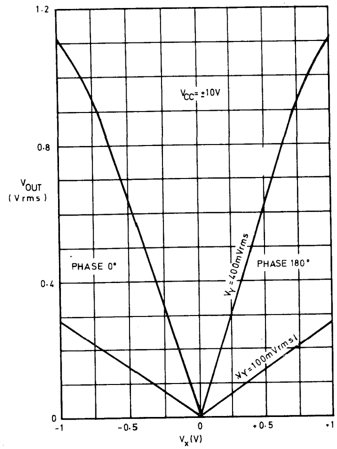


Fig. 5 Transfer characteristics in multiplier mode

PLESSEY
SEMICONDUCTORS

TELECOMMUNICATIONS CIRCUITS

SL1030C

200MHz WIDEBAND AMPLIFIER

The SL1030 is a silicon integrated circuit designed for use as a general purpose very wideband amplifier. External components enable users to tailor the characteristics of the amplifier for particular applications. The gain can be selected between 20 and 60dB; the input impedance can be 50Ω, 75Ω or 1kΩ, and the compromise between current consumption and output swing can be selected by the external components.

A regulator is provided on the chip, enabling supply voltages from 8 to 15 volts to be used with no variation in characteristics. Alternatively, the regulator can be bypassed and supplies from 4.0 to 10 volts used.

The amplifier is protected against damage from input voltage transients and is stable when driving capacitive and inductive loads.

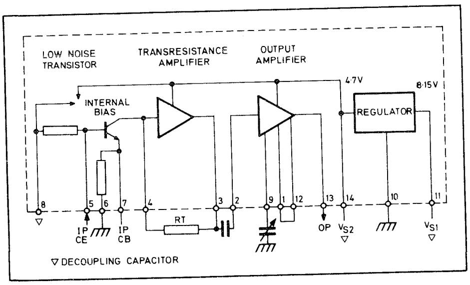


Fig. 1 General schematic

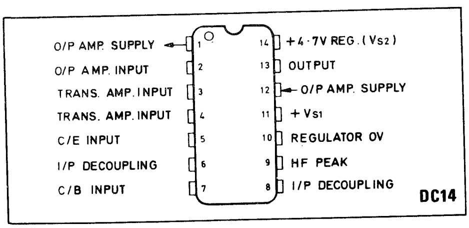


Fig. 2 Pin connections (top)

FEATURES

- Bandwidth up to 200 MHz
- Low Noise
- Single Supply
- Input Impedance Adjustable – 50Ω, 75Ω or 1kΩ
- Gain Programmable between 20dB and 60dB
- Drives Capacitive or Inductive Loads

APPLICATIONS

- Wideband Pulse Amplifiers
- Frequency Selective IF Amplifiers
- Low Noise Preamplifiers

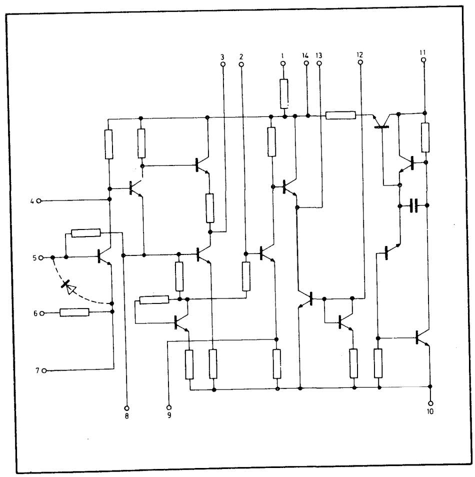


Fig. 3 Circuit diagram

QUICK REFERENCE DATA

Supply Voltage	+4V to +15V
Supply Current at V_S = 10V	20 mA (Typ.)
Voltage Gain at 100 MHz	40dB (Typ.)
Noise Figure at 100 MHz, R_S = 50Ω	3dB (Typ.)
Second Order Intermodulation Distortion	–50dB (Typ.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} 22°C ± 2°C
V_{S1} 10V
R_1 = 1 kilohm
R_2 = 32 kilohms

Characteristic	Test Cct.	Value Min.	Value Typ.	Value Max.	Units	Conditions
Voltage gain	A	28	30	32	dB	f = 100 MHz
	B	37	40	43	dB	" " "
Gain flatness			± 0.5		dB	f = 10 kHz to 150 MHz (Note 1)
Noise figure	A		6.5	8.0	dB	f = 100 MHz, R_S 50Ω
	B		3.0	4.5	dB	
Gain compression	A		0.2	1.0	dB	f = 100 MHz, load impedance = 50Ω P_{out} = 0dBm
Output voltage	B		1		V pk/pk	f = 10 MHz, load impedance = 100Ω
Rise time	B		3		ns	V_{out} = 1.0 V pk/pk
Input VSWR	A		1.2			f = 10 kHz to 150MHz w.r.t. 50Ω
Supply current			20	30	mA	V_{S1} = 10V or V_{S2} = 5V
Regulation $\Delta V_{S2}/\Delta V_{S1}$			1	5	%	V_{S1} = 10V to 15V
Intermodulation distortion						
2nd order	A		−50		dB*	P_{out} = 0dBm (Note 2), V_{S2} = 10V
3rd order	A		−60		dB*	
Harmonic distortion						
2nd harmonic	A		−30		dB*	f = 100 MHz, P_{out} = 0dBm, V_{S2} = 10V, R_L = 50Ω
3rd harmonic	A		−40		dB*	
Input impedance						
Common base			16		Ω	f < 10 MHz
Common emitter			1		kΩ	" "

NOTES

1. The gain flatness is dependent on layout and on the value of the peaking capacitor. See OPERATING NOTES for details.
2. In each of two tones at 10 and 10.5 MHz, R_L = 50Ω

* Referred to output.

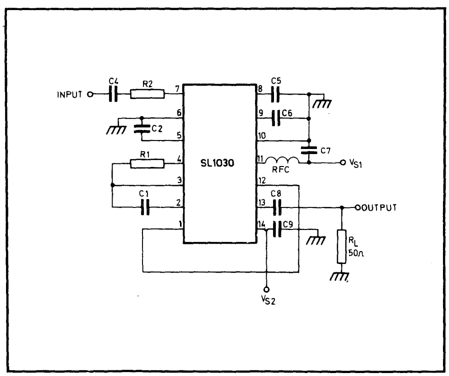


Fig. 4 Test circuit A – common base

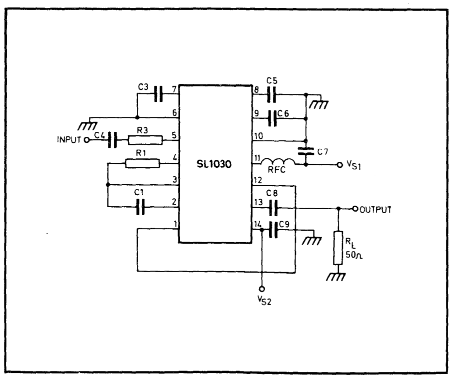


Fig. 5 Test circuit B – common emitter

TYPICAL ELECTRICAL CHARACTERISTICS

The following conditions apply to the characteristics given in Figs. 6 to 16 unless otherwise stated:

Free air temperature	22°C
Load resistance	50Ω
R_T	1 kΩ

Intermodulation products (Fig. 6) are measured with specified output power in each of two tones at 10 MHz and 10.5 MHz.

The values for C_P quoted in Figs. 12 and 13 were selected with R_L = 50Ω but will vary with load impedance and circuit layout.

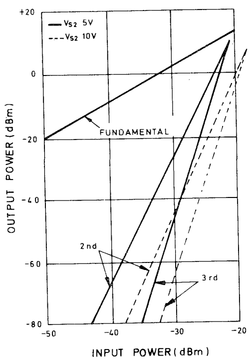


Fig. 6 Intermodulation products

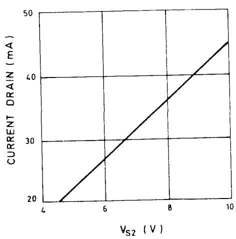


Fig. 7 Supply current v. unreg. supply voltage

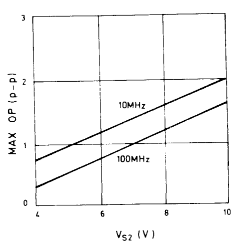


Fig. 8 Max o/p voltage v. unreg. supply voltage

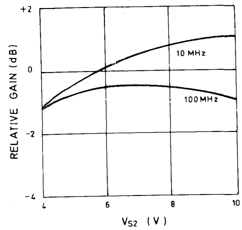


Fig. 9 Common base gain v. unreg. supply voltage

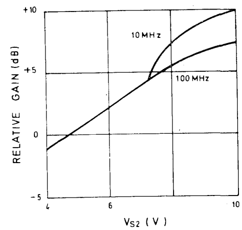


Fig. 10 Common emitter gain v. unreg. supply voltage

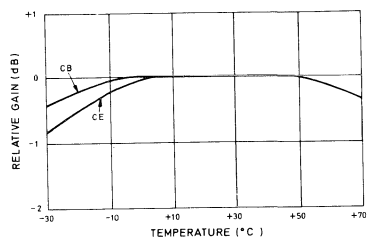


Fig. 11 Gain v. temperature

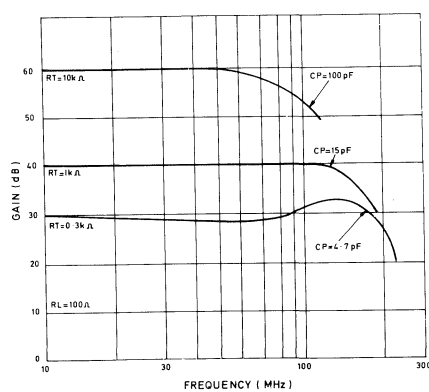


Fig. 12 Common emitter gain v. frequency

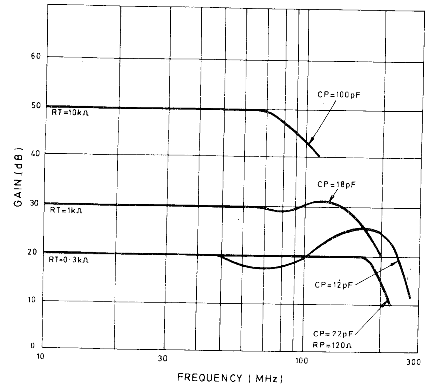


Fig. 13 Common base gain v. frequency

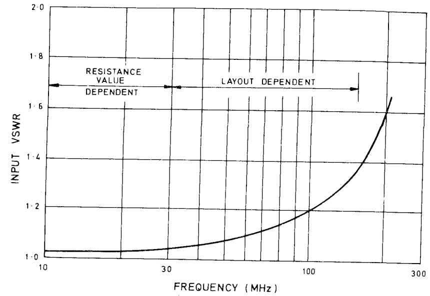


Fig. 16 Input VSWR v. frequency

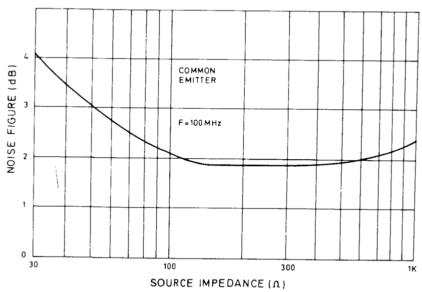


Fig. 14 Noise figure v. source impedance

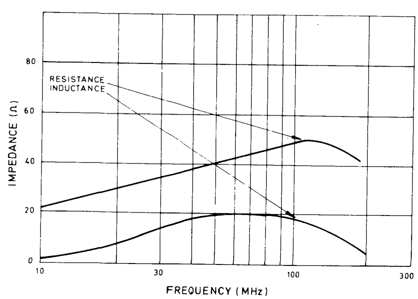


Fig. 15 Output impedance v. frequency

OPERATING NOTES

Low Noise Input Stage

As shown in Fig. 1, the input transistor can be used in common base or common emitter by using either pin 7 or pin 5 as the input, the other pin being decoupled. If a well-defined 50 or 75Ω input impedance is required, then a circuit similar to test circuit A (Fig. 4) should be used. An accuracy of ± 5% can be expected in the input impedance of this circuit since the input impedance of the common base stage is very reproducible and also is to some extent masked by the external resistor. A return loss of 30dB up to 100 MHz can be achieved with careful layout and the use of a physically small, accurate external resistor. The value of the resistor should be 56Ω for 75Ω input impedance and 33Ω if 50Ω input impedance is required.

The noise figure of this transistor is flat from the flicker noise knee around 10 Hz to over 150 MHz.

Transresistance Amplifier

The transresistance amplifier will operate correctly for values of R_T from 200Ω to 10 kΩ. The voltage gain of the complete amplifier is of course directly proportional to R_T. See Figs. 12 and 13.

Output Stage

When the internal regulator is bypassed for applying the supply voltage to pin 14, some control of the quiescent current is possible. The biasing circuitry has been designed so that the individual currents track together with the supply voltage and with each other. This enables a significant improvement to be made in the output swing into low impedance loads at the expense of increased current consumption. See Fig. 7. The quiescent current of the first device also increases, giving an increase in gain in the common emitter configuration. The quiescent current in the output stage can be varied by means of an external resistor. The link between pins 1 and 12 must be removed and a resistor added between pins 14 and 12. The current is 10 mA with 2.5 kΩ and is approximately inversely proportional to the resistor value.

Peaking Capacitor C_P

The frequency response of the amplifier is dominated by the output emitter follower which begins to roll off at about 50 MHz. The high frequency peaking capacitor is used to compensate for this roll-off and also that due to stray inductance and capacity in the external circuitry. The values of peaking capacitor used in the test circuits have been selected for best gain flatness in the test fixture but are not necessarily typical of the values required in different layouts since the stray reactances associated with a plug-in test facility are inevitably higher than in a directly wired circuit. The typical curves were measured with an SL1030 directly soldered into a PC board and the values of the peaking capacitor given will be more typical of the normal situation.

Layout and Stability

Since gains of 40dB are available up to VHF frequencies normal high frequency layout precautions are necessary with respect to grounding and decoupling. Decoupling capacitors should be low inductance ceramic types (Erie Weecons are ideal) and to ensure good earth connections a continuous ground plane should be provided around and underneath the circuit. Decoupling of pins 5 or 7 is critical and inadequate decoupling of pin 14 can cause instability. Since no overall feedback is used, the amplifier is very tolerant of load reactance and no instability has been observed even with pure capacitive loads. A certain amount of care is needed when using the internal regulator. If the decoupling on pin 11 is effective above 200 MHz, then instability can occur within the regulator. This can be completely stopped by inserting an inductance of a few hundred nanohenries between the decoupling capacitor and pin 11 as shown on the test circuits.

ABSOLUTE MAXIMUM RATINGS

V_{S1} (Pin 11)	+15V
V_{S2} (Pin 14)	+10V
Storage temperature	−55°C to +150°C
Operating temperature (ambient)	−55°C to +125°C

PLESSEY
SEMICONDUCTORS

SL1202C SL1203C

LOW NOISE PREAMPLIFIERS

The SL1202C and SL1203C are monolithic silicon integrated circuits designed primarily for use as a low noise preamplifiers in infra-red systems. Their exceptional noise performance and high gain make these amplifiers suitable for use in systems requiring low noise amplification from a source in the range 30Ω to 120Ω. The circuit can be divided into two sections. A single-ended IN/single-ended OUT low noise preamplifier and a single-ended IN, balanced OUT post amplifier. The preamplifier alone is available in an 8-lead TO5 encapsulation as the SL1202C and the preamplifier plus post amplifier in a 16-lead DIL, as the SL1203C. The input transistor has a base resistance of less than 20Ω, enabling very good noise performance to be achieved from low impedance sources. The balanced output stage has adjustable quiescent current which gives the user the facility of minimising power consumption within the limit imposed by driving the required output voltage into the specified load impedance. This load impedance can be as low as 50Ω. The gain of the preamplifier can be set in the range 35 to 57 dB by an external resistor.

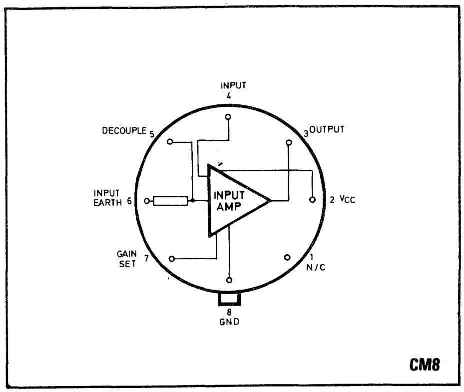


Fig. 1 Block diagram of SL1202C

FEATURES

- Gain: 35 to 67 dB (Set by external components)
- Bandwidth: 3.6 MHz
- Input Impedance: 2kΩ
- Equivalent Input Noise: (R_S = 50Ω) 0.9 nV/√Hz
- Low I/F Noise
- Balanced Output Stage
- Low Power Consumption

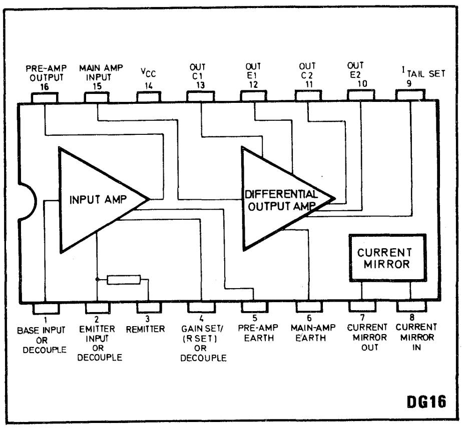


Fig. 2 Block diagram of SL1203C

ABSOLUTE MAXIMUM RATINGS

V_{CC}	+10V
Operating temperature	−55°C to +125°C
Storage temperature	−55°C to +150°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

V_{CC} = +6V
Source resistance = 50Ω
T_{amb} = 25°C
Load impedance (i) SL1202 = 1MΩ (ii) SL1203 = 100Ω balanced

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Upper cut-off frequency (−3dB)	Both	2.5	3.6		MHz	
Input impedance	Both		2.0		kΩ	
Output impedance	SL1202		80		Ω	
	SL1203	See operating note 1				
Voltage gain	SL1202	52	57	62	dB	R_{set} = 0
	SL1202		35		dB	R_{set} = 6kΩ
	SL1203	62	67	72	dB	R_{set} = 0
	SL1203		37		dB	R_{set} = 20kΩ
Output voltage	SL1202	2.5	3.5		Vp-p	R_{set} = 0
	SL1202		1.0		Vp-p	R_{set} = 6kΩ
	SL1203	0.4	0.7		Vp-p	R_{set} = 0, see operating note 1
	SL1203		0.6		Vp-p	R_{set} = 20kΩ see operating note 1
Equivalent input noise voltage	Both		0.9	1.2	nV/√Hz	R_S = 50Ω
Supply current	SL1202		3	5	mA	
	SL1203		20	30	mA	See operating note 1

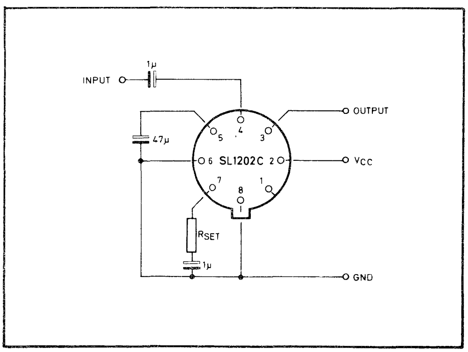


Fig. 3 SL1202C test circuit

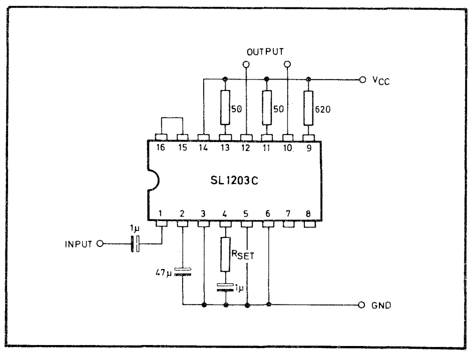


Fig. 4 SL1203C test circuit

TYPICAL ELECTRICAL CHARACTERISTICS (Figs. 5, 6 & 7)

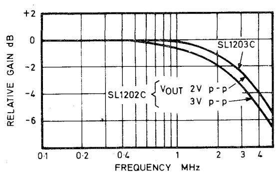


Fig. 5 Frequency response

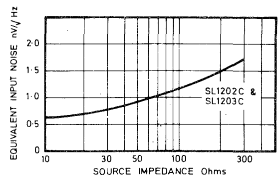


Fig. 6 Equivalent input noise v. source impedance

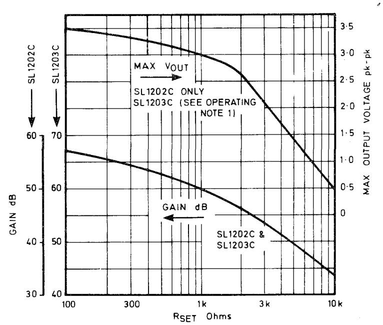


Fig. 7 Max. output voltage and gain v. R_{set}

OPERATING NOTES

1. The Output Amplifier (SL1203C)

This consists of two cascaded differential stages, and is primarily intended for driving a balanced 100Ω load (Pins 11 and 13). The tail current of the output stage may be increased from its preset value of 1 mA by connecting a resistor between Pins 9 and 14. The maximum output swing is determined by the value of the output stage tail current, up to a 1.0 volt peak-to-peak differential maximum. This resistor should be not less than 500Ω to avoid exceeding the current ratings of the transistors.

The output swing available, and the external resistor between Pins 9 and 14 are related by the expression:

$$5V_{swing} = \frac{V_{SS} - 0.75}{\frac{R.10}{10+R} + 0.75}$$

where V is in volts, R is in kΩ

e.g. for R = 1kΩ, V_{SS} = 6.0 volts

$$V_{swing} = \frac{5.25}{5 \times 1.74} = \mathbf{600mV}$$

for R = ∞, V_{SS} = 6.0 volts

$$V_{swing} = \frac{5.25}{5 \times 10.75} = \mathbf{100mV}$$

Asymmetric limiting, caused by differential output offsets, may reduce the usable swing below the theoretical maximum. Offset may be trimmed out by means of a resistor between Pin 16 and ground (or V_{SS}). The specifications for output swing of the SL1203C apply to untrimmed units.

Varying R_{set} reduces the output swing capability of the SL1202C as shown in the typical electrical characteristics. The output swing of the SL1203C is unaffected by R_{set} for values less than 20 kΩ. Hence a gain reduction of 30 dB can be obtained without degrading the output swing capability.

2. Input Stage

The input is uncommitted and may be arranged as common base or common emitter. Common emitter gives the highest input impedance, and thus the lowest value of input coupling capacitor for a given LF response. This is the configuration described in this data sheet. However, the common base configuration can also have certain advantages, for example a CMT detector can be directly coupled into the amplifier – the quiescent current of the first stage then provides detector bias.

3. Current Mirror

Included in the SL1203C is an NPN current mirror with 2:1 scaling (Pins 7 and 8); a bias supply for CMT infra-red detectors. The mirror is tied to the output amplifier ground rail, and thus can only be used when the output amplifier is powered.

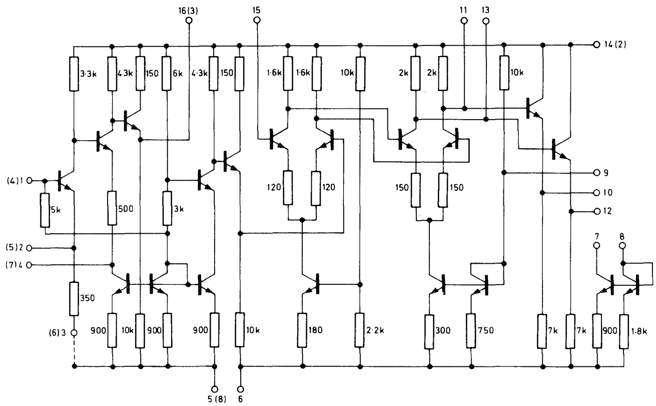


Fig. 8 Circuit diagram of SL1202C/SL1203C. (Pin numbers are shown thus: (4)-SL1202C, 4-SL1203C.)

PLESSEY
SEMICONDUCTORS

SL1205C

LOW NOISE PREAMPLIFIER

The SL1205 is a monolithic integrated circuit designed specifically for use in infra-red systems as a low-noise preamplifier interfacing with a CMT detector.

To reduce physical size, the SL1205 is encapsulated in a TO-71 package; in addition, this design minimises the number and size of external capacitors required.

The 6.5MHz-wide bandwidth enables fully TV-compatible video response to be obtained. In such systems it is envisaged that the sweep-out mode of detector operation will be used.

Applications in other systems are not precluded: the amplifier has an input impedance of 2kΩ, an output impedance of about 50Ω and an optimum noise performance from low impedance sources (~100Ω). Power consumption is very low: 10mW at V_{cc} = 5.0 volts, and only a single positive power supply is required.

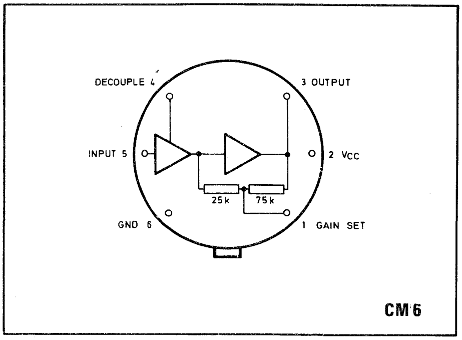


Fig. 1 Pin connections (viewed from the top)

FEATURES

- Gain 49-59dB
- Bandwidth 6.5MHz
- Equivalent Input Noise Voltage 0.8nV/√Hz
- Low IF Noise
- Small Encapsulation (TO-71)
- Minimum External Components
- Low Power Consumption

QUICK REFERENCE DATA

- Supply Voltage 5 to 9V
- Supply Current 1.8mA Typ.
- Upper Cut-Off Frequency 5 MHz Min.

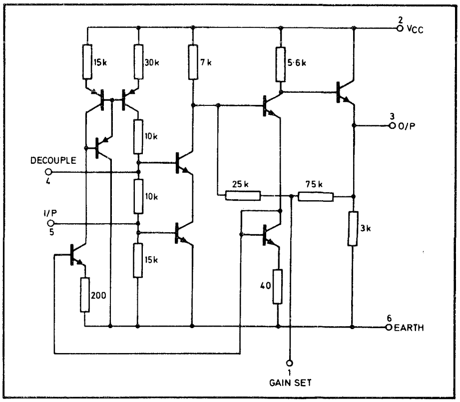


Fig. 2 Circuit diagram

OPERATING NOTES

Noise Performance

The noise performance of the SL1205 is optimum for source impedances in the range 20 to 150Ω. The quiescent current of the input transistor is approximately 0.5mA and its base resistance is 20Ω. The operating current has been chosen to give a high input impedance, hence reducing the value of input coupling capacitor required without a large degradation in noise performance. Flicker noise is not normally a problem, the knee frequency being below 100Hz.

Output Voltage

The maximum output voltage before clipping is guaranteed at 1.5V min. at V_{CC} = 5 volts into a 10kΩ. in parallel with 5 pF load. Larger output voltages can be obtained by increasing the supply voltage. Driving low impedance or capacitive loads is eased by increasing the quiescent current of the output emitter follower, achieved by connecting an external resistor between pin 3 and earth. The resistor should be greater than 200Ω to avoid exceeding the ratings of the output transistor.

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

$V_{CC} = 5.0V$
$T_{amb} = +25°C$
Source Resistance = 50 Ω
Load Impedance = 10k Ω in parallel with 5pF

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions
Voltage gain	56	59	62	dB	$R_{set} = \infty$
		48			$R_{set} = 0$
Equivalent Input Noise Voltage		0.8	1.2	$nV/\sqrt{Hz}$	$R_{set} = \infty$
		0.8		$nV/\sqrt{Hz}$	$R_{set} = 0$
Output voltage	1.5	2.0		V p-p	
Supply current		1.8	3.0	mA	
Output resistance		50		Ω	
Input resistance		2		k Ω	
Input capacitance		15		pF	
Upper cut-off frequency	5	6.5		MHz	$V_{out} = 10mV$ p-p
		6.2		MHz	$V_{out} = 1.5V$ p-p

ABSOLUTE MAXIMUM RATINGS

V_{cc} (pin 2 wrt ground) 10.0V
Storage Temperature −55°C to +150°C
Operating Temperature −55°C to +125°C

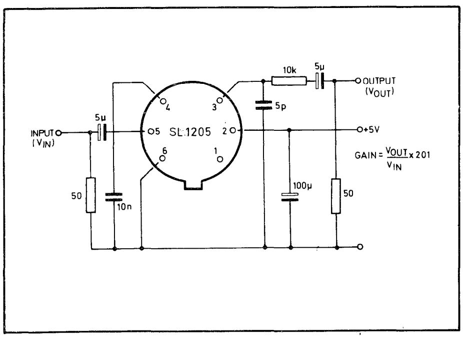


Fig.3 Test circuit

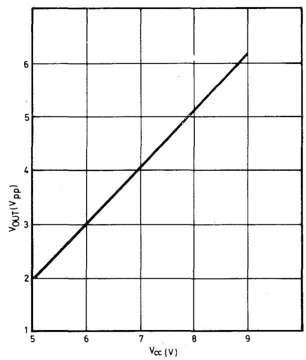


Fig.4 Output voltage v. supply voltage

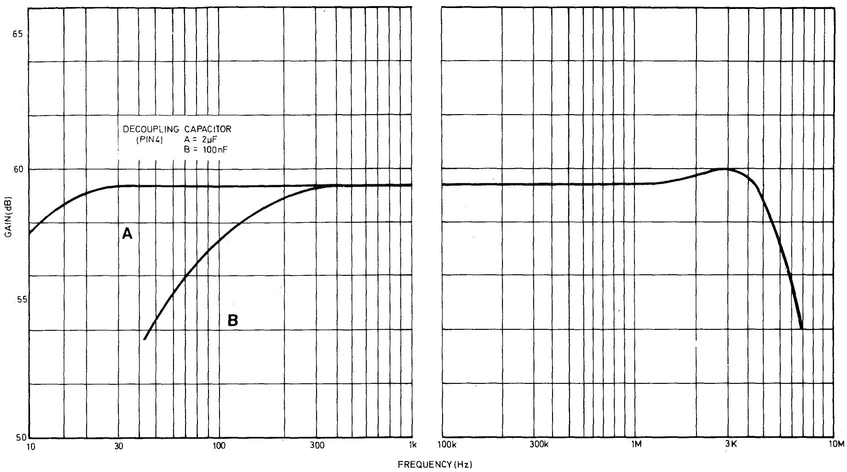


Fig.5 Gain v. frequency

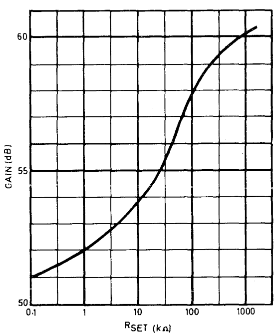


Fig.6 Gain v. R_{set}

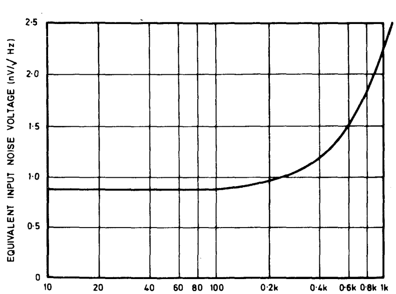


Fig.7 Noise characteristic

TYPICAL APPLICATIONS

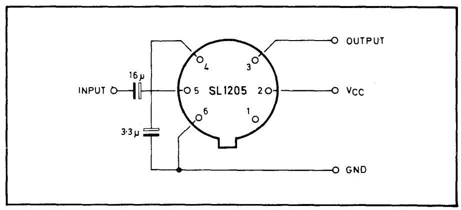


Fig.8 Gain 60 dB (fixed), frequency response 5Hz to 6.5MHz

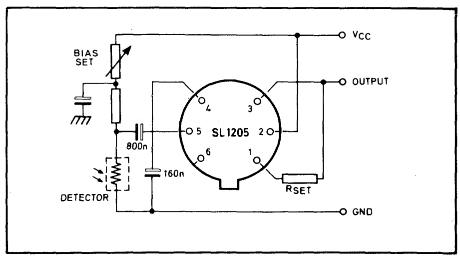


Fig.9 Gain 50 to 60 dB (set by R set),
frequency response 100Hz to 6.5MHz, CMT detector.

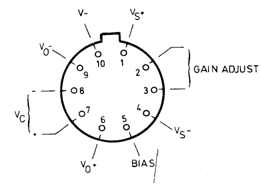
PLESSEY SEMICONDUCTORS

TELECOMMUNICATIONS CIRCUITS

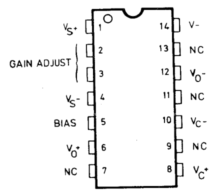
SL1496C SL1596C

DOUBLE-BALANCED MODULATOR/DEMODULATOR

The SL1596C and SL1496C are versatile monolithic integrated circuit double balanced modulators/demodulators, designed for use where the output voltage is the product of the signal input voltage and the switching carrier voltage. The SL1596 has an operating temperature range of –55°C to +125°C, whilst that of the SL1496 is 0°C to +70°C.



CM10



DG16 DP16

FEATURES

- Carrier Suppression 65dB Typ. @ 500 kHz; 50dB Typ. @ 10 MHz
- Common Mode Rejection 85dB Typ.
- Gain and Signal Handling Both Adjustable
- Balanced Inputs and Outputs

APPLICATIONS

- DSB, DSBSC, AM Modulation
- Synchronous Detection
- FM Detection
- Phase Detection
- Telephone FDM Systems

ORDERING CODES

SL1496C — CM, SL1496C — DG, SL1496C — DP
SL1596C — CM, SL1596C — DG

ABSOLUTE MAXIMUM RATINGS
(Pin number reference to CM package)

Applied voltage*	30V
Differential input signal (V_7—V_8)	±5V
Differential input signal (V_4—V_1)	± $(5+I_5R_E)$V
Bias current (I_5)	10mA
Operating temperature range	
SL1496	0 °C to +70 °C
SL1596	—55 °C to +125 °C

CM Package

Storage temperature range	—55 °C to +175 °C
Junction temperature	+175 °C
Package dissipation (25 °C)	680mW

DG Package

Storage temperature range	—55 °C to +175 °C
Junction temperature	+175 °C
Package dissipation (25 °C)	600mW

DP Package

Storage temperature range	—55 °C to +125 °C
Junction temperature	+125 °C
Package dissipation (25 °C)	500mW

* Voltage between pins 6-7, 8-1

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):—
$V^+ = +12V$ DC, $V^- = -8V$ DC, $I_5 = 1.0$ mA DC, $R_L = 3.9$ kΩ, $R_e = 1.0$ kΩ $T_A = +25°C$
All input and output characteristics single-ended, unless otherwise stated.

Characteristic*	SL1596 Min	SL1596 Typ	SL1596 Max	SL1496 Min	SL1496 Typ	SL1496 Max	Units
Carrier Feedthrough							µV(rms)
V_C = 60 mV(rms) sinewave and offset adjusted to zero, f_C = 1.0 kHz	—	40	—	—	40	—	
f_C = 10 MHz	—	140	—	—	140	—	
V_C = 300 mVp-p square wave							mV(rms)
offset adjusted to zero, f_C = 1.0 kHz	—	0.04	0.2	—	0.04	0.4	
offset not adjusted, f_C = 1.0 kHz	—	20	100	—	20	200	
Carrier Suppression							dB
f_S = 10 kHz, 300 mV(rms)							
f_C = 500 kHz, 60 mV(rms) sinewave	50	65	—	40	65	—	
f_C = 10 MHz, 60 mV(rms) sinewave	—	50	—	—	50	—	
Signal Gain V_S = 100 mV(rms), f = 1.0 kHz; $\lvert V_C \rvert$ = 0.5 V DC	2.5	3.5	—	2.5	3.5	—	V/V
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz							
Parallel Input Resistance	—	200	—	—	200	—	kΩ
Parallel Input Capacitance	—	2.0	—	—	2.0	—	pF
Single-Ended Output Impedance, f = 10 MHz							
Parallel Output Resistance	—	40	—	—	40	—	kΩ
Parallel Output Capacitance	—	5.0	—	—	5.0	—	pF
Input Bias Current $\frac{I_1 + I_4}{2}$; $\frac{I_7 + I_8}{2}$	—	12	25	—	12	30	µA
Input Offset Current $(I_1 - I_4)$, $(I_7 - I_8)$	—	0.7	5.0	—	0.7	7.0	µA
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	—	2.0	—	—	2.0	—	nA/°C
Output Offset Current $(I_6 - I_9)$	—	14	50	—	14	80	µA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	—	90	—	—	90	—	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	—	5.0	—	—	5.0	—	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C \rvert$ = 0.5 V DC	—	−85	—	—	−85	—	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	—	8.0	—	—	8.0	—	V DC
Differential Output Voltage Swing Capability	—	8.0	—	—	8.0	—	Vp-p
Power Supply Current							mA DC
$I_6 + I_9$	—	2.0	3.0	—	2.0	4.0	
I_{10}	—	3.0	4.0	—	3.0	5.0	
DC Power Dissipation	—	33	—	—	33	—	mW

*Pin numbers are given for TO-5 package.

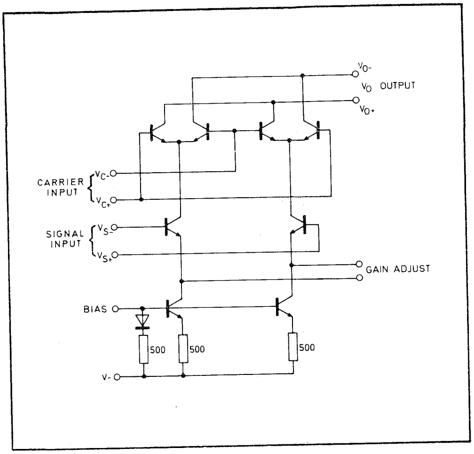


Fig. 2 ***Circuit diagram***

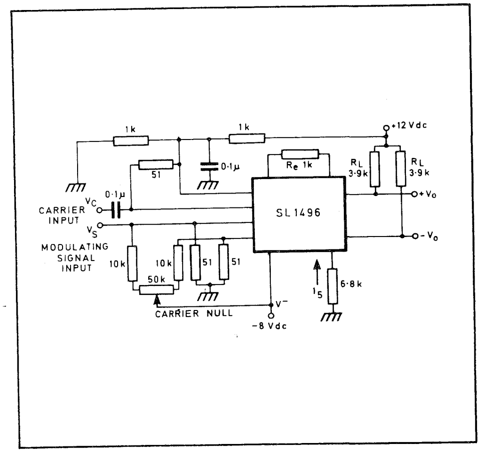


Fig. 3 ***Typical modulator circuit***

PLESSEY SEMICONDUCTORS

SL1521 SERIES
LIMITING RF AMPLIFIERS

SL1521, A, B & C
WIDEBAND AMPLIFIERS

The SL1521A, B and C are wide band amplifiers intended for use in successive detection logarithmic IF strips operating at centre frequencies of up to 200MHz. It is a plug in replacement for the SL521 series of RF amplifiers. The mid-band voltage gain of the SL1521 is typically 12dB. The SL1521 A, B and C differ mainly in the tolerance of voltage gain.

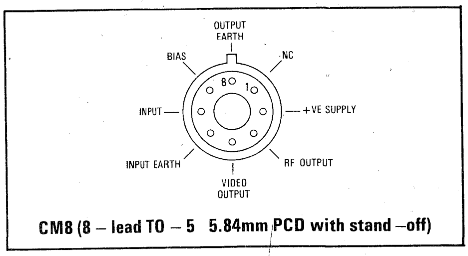


Fig. 1 Pin connections

APPLICATIONS

- Radar IF Strips
- Wideband Amplification

ABSOLUTE MAXIMUM RATINGS
(Non-simultaneous)

Storage temperature range	−55°C to +175°C
Operating temperature range	−55°C to +125°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	300°C/W
Chip-to-case thermal resistance	95°C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	+9V

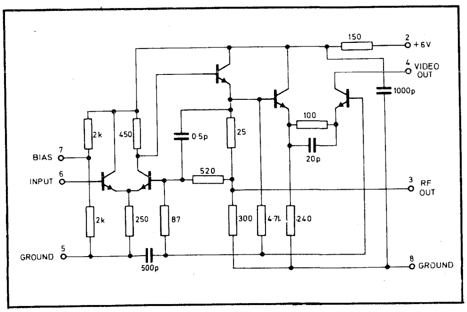


Fig. 2 Circuit diagram

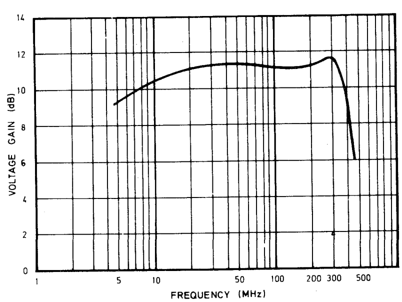


Fig. 3 Voltage gain v. frequency

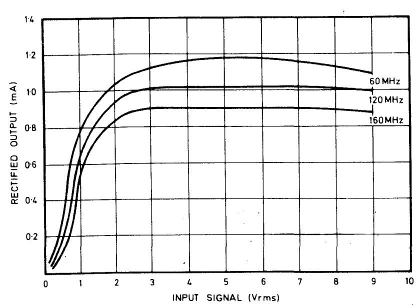


Fig. 4 Rectified output current v. input signal

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature = +22°C ±2°C
Supply voltage = +5.2V
DC connection between input and bias pins.

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain, f = 120 MHz	SL1521 A	11.5		12.5	dB	
	SL1521 B	11.2		12.8	dB	3mVrms input
	SL1521 C	10.8		13.1	dB	50 ohms source
Voltage gain, f = 160MHz	SL1521 A	11.2		12.8	dB	4pF load + 500 Ω
	SL1521 B	11.0		13.0	dB	
	SL1521 C	10.6		13.4	dB	
Upper cut-off frequency	SL1521 A	315	350		MHz	
	SL1521 B	315	350		MHz	50 ohms source
	SL1521 C	300	350		MHz	
Lower cut-off frequency	All types		6	10	MHz	50 ohms source
Propagation delay	All types		0.6		ns	
Maximum rectified video output current	SL1521 A	0.95		1.05	mA	f = 120 MHz
	SL1521 B	0.90		1.10	mA	0.5Vrms input
	SL1521 C	0.90		1.20	mA	4pF load, no RL
Variation of gain with supply voltage	All types		1.0		dB/V	
Variation of maximum rectified output current with supply voltage	All types		30		%/V	
Maximum input signal before overload	All types		1.5		V rms	See note below
Noise figure			3	4.5	dB	f = 120 MHz, source resistance optimised
Supply current	All types	10.0	15.0	20.0	mA	
Maximum RF output voltage	All types	1.0			Vp-p	

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction to TR1 on peaks.

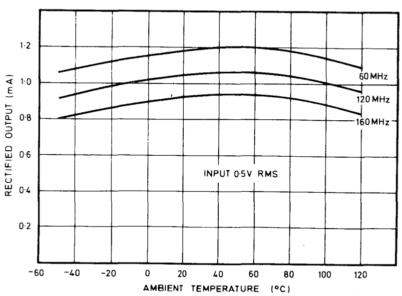


Fig. 5 Maximum rectified output current v. temperature

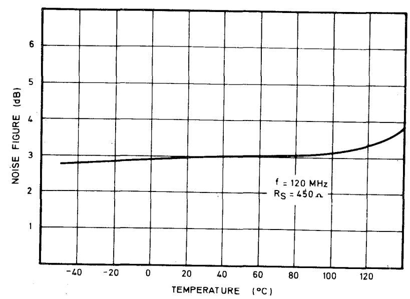


Fig. 6 Typical noise figure v. temperature

Operating Notes

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rises times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

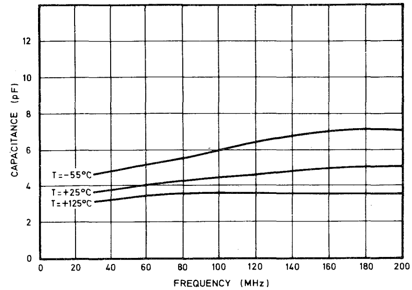


Fig. 7 Input admittance with open-circuit output

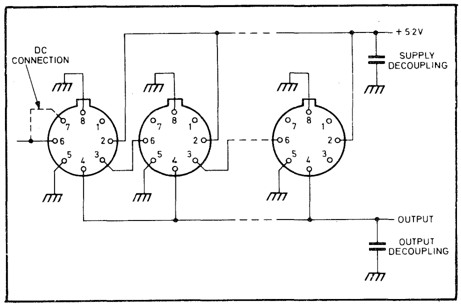


Fig. 8 Direct coupled amplifiers

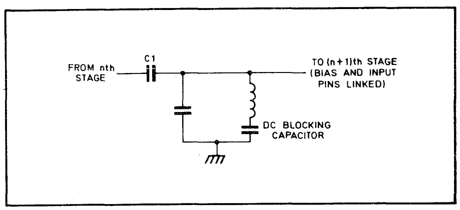


Fig. 9 Suitable interstage tuned circuit

PLESSEY
SEMICONDUCTORS

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1610C, SL1611C & SL1612C
RF/IF AMPLIFIERS

The SL1610C and SL1611C are low noise, low distortion, RF voltage amplifiers with integral supply line decoupling and AGC facilities. The SL1610C has a voltage gain of 10 and a bandwidth of 140MHz, while the SL1611C has a voltage gain of 20 and a bandwidth of 100MHz. Both circuits have a 50dB AGC range with maximum signal handling of 250mV rms. As they are voltage amplifiers they have high input impedance and low output impedance.

The SL1612C is a low noise, low distortion, IF voltage amplifier similar to the SL1610C and SL1611C but having a voltage gain of 50, a bandwidth of 15MHz and only 20mW power consumption. It has a 70dB AGC range with maximum signal handling of 250mV rms.

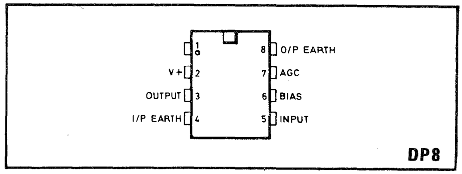


Fig. 1 Pin connections (top view)

APPLICATIONS

- IF Amplifiers
- RF Amplifiers
- AGC-Controlled Amplifiers

FEATURES

- Low Noise
- Low Distortion
- 1V rms Output
- Wide AGC Range
- On-Chip Decoupling

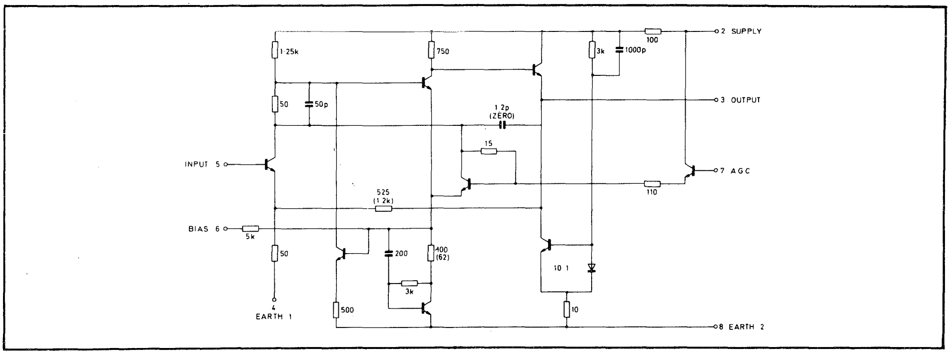


Fig. 2 Circuit diagram of SL1610C and SL1611C
(Component values for SL1611C are shown in brackets)

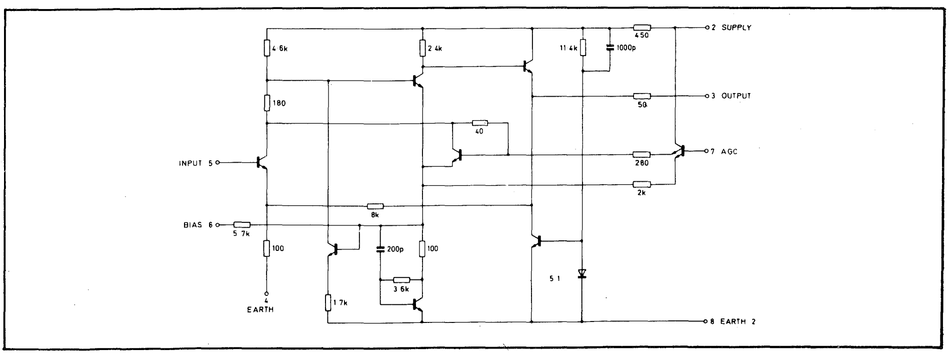


Fig. 3 Circuit diagram of SL1612C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage = 6V
Temperature = +25°C (unless otherwise stated)
Pins 5 and 6 strapped together
AGC not applied unless specified.

Characteristic	Circuit	Typical Value	Units	Test conditions
Voltage gain (see note1)	SL1610C	20	dB	30MHz; Source = 25Ω
	SL1611C	26	dB	30MHz; Load R ⩾ 500Ω
	SL1612C	34	dB	1.75MHz; Load C ⩽ 5pF
Cut-off frequency (−3dB) (See Fig. 9 and note1)	SL1610C	120	MHz	Source = 25Ω
	SL1611C	80	MHz	Load R ⩾ 500Ω
	SL1612C	12	MHz	Load C ⩽ 5pF
Noise Figure	SL1610C	4	dB	Source = 300Ω, f = 30MHz
	SL1611C	4	dB	Source = 300Ω, f = 30MHz
	SL1612C	3	dB	Source = 800Ω, f = 1.75MHz
Max. input signal (1% cross modulation) No AGC applied	SL1610C	100	mVrms	Load 150Ω, f = 10MHz
	SL1611C	50	mVrms	Load 150Ω, f = 10MHz
	SL1612C	20	mVrms	Load 1.2kΩ, f = 1.75MHz
Max. input signal (1% cross modulation) Full AGC applied	SL1610C	250	mVrms	f = 10MHz
	SL1611C	250	mVrms	f = 10MHz
	SL1612C	250	mVrms	f = 1.75MHz
AGC range (See Fig 10)	SL1610C	50	dB	
	SL1611C	50	dB	
	SL1612C	70	dB	
AGC current	SL1610C	0.15	mA	AGC Voltage = 5.1V
	SL1611C	0.15	mA	
	SL1612C	0.15	mA	
Quiescent current consumption	SL1610C	15	mA	Output open circuit
	SL1611C	15	mA	
	SL1612C	3.3	mA	

NOTE
1. Gain and frequency response of these circuits are relatively independent of supply voltage within the range 6 to 9V

OPERATING NOTES

The SL1610C, SL1611C and SL1612C are normally used with pins 5 and 6 strapped. A slight improvement in noise figure, and an increase in the input impedance, may be obtained by feeding the device from a coil or tuned circuit, bias from pin 6 being decoupled and applied to one end of the coil and the signal being taken either from the other end or from a tap.

The characteristics of these units have been expressed in G parameters which are defined as shown in Fig. 4.

These parameters correspond to the normal operation of a voltage amplifier which is usually operating into a load much higher than its output impedance and from a source much lower than its input impedance. Hence the input admittance (G_{11}) and voltage gain (G_{21}) are measured with open circuit output, and the output impedance (G_{22}) with short circuit input. The parasitic feedback parameter is the current transfer (G_{12}) i.e. the current which flows in a short circuit across the input for a given current flowing in the output circuit.

Since the effects of G_{12} are small for reasonable values of load and source impedance, the approximate equivalent circuit given in Fig. 5 may be used.

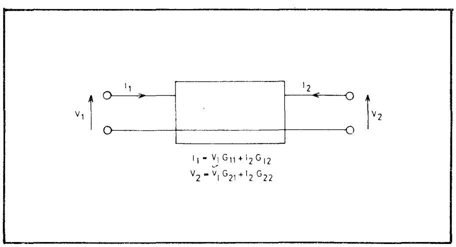


Fig. 4 Definition of G parameters

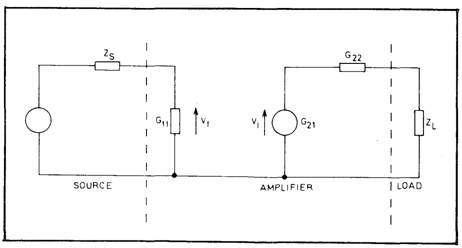


Fig. 5 Amplifier equivalent circuit

Hence the typical effects of applying finite load and source impedances, real or complex, may be evaluated by the use of the graphs showing the values of the major parameters versus frequency. At lower frequencies the limitation on Z_L is dependent upon output signal; for maximum output $Z_L = 100\Omega$.

Stability

Both the input admittance G_{11} and the output impedance G_{22} have negative real parts at certain frequencies. The equivalent circuits of input and output are shown in Fig. 6 and the values of R_{in}, R_{out}, C_{in} and L_{out} may be determined for any particular frequency from the graphs Fig. 7 and 8. It will be seen that, for the SL1610C and the SL1611C R_{in} is negative between 30 and 100MHz, and R_{out} is negative over the whole operating frequency range. For the SL1612C, R_{in} is not negative and R_{out} is negative only below 700KHz.

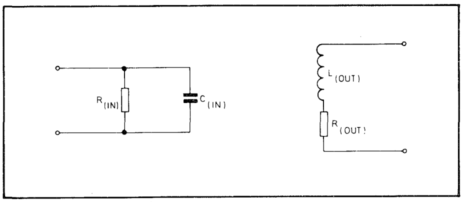


Fig. 6 Input and output equivalent circuits

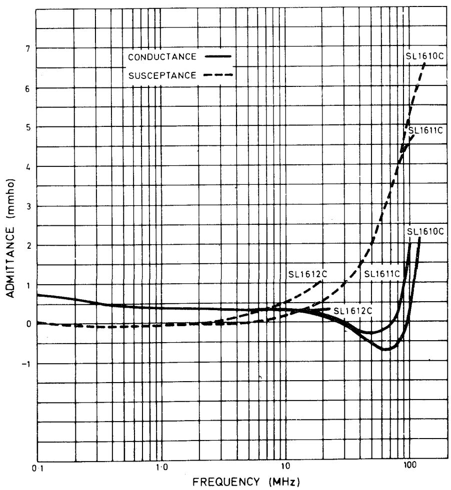


Fig. 7 Input admittance with O/C output (G_{11})

It is evident that if an inductive element having inductance L1 and parallel resistance R1 is connected across the input, oscillation will occur if R_{in} is negative at the resonant frequency of C_{in} and L1, and R1 is higher than R_{in}.

Similarly, if a capacitor C1 in series with a resistance R2 is connected across the output oscillation will occur if, at the resonant frequency of L_{out} and C1, R_{out} has a negative resistance greater than the positive resistance R2. Where the input may be inductive, therefore, it may be shunted by a resistor and where the load may be capacitive 47Ω should be placed in series with the output.

These devices may be used with supplies up to +9V with increased dissipation.

The AGC characteristics shown in Fig. 8 vary somewhat with temperature: a preset potentiometer should not, therefore, be used to set the gain of either of these circuits if accurate gain is required.

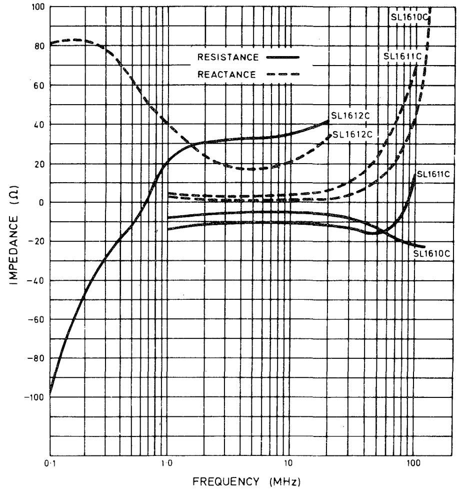


Fig. 8 Output impedance with S/C input (G_{22})

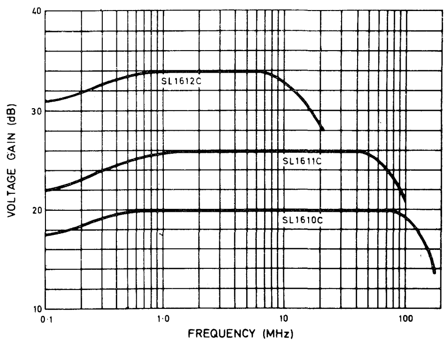


Fig. 9 Voltage gain (G_{21})

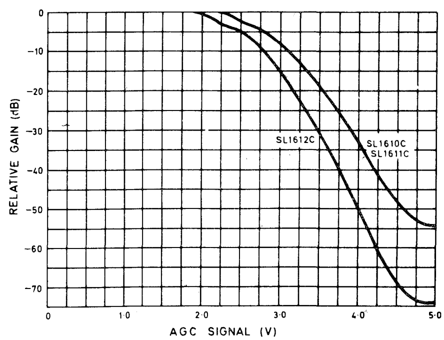


Fig. 10 AGC characteristics

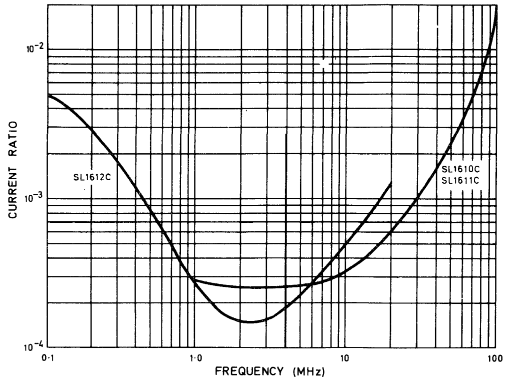


Fig. 11 Reverse current transfer ratio (G_{12})

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−30°C to + 85 °C
Supply voltage	+10V.
Operating temperature	−30°C to +70°C

PLESSEY
SEMICONDUCTORS

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1613C

LIMITING AMPLIFIER/DETECTOR

The SL1613C is a low noise limiting amplifier intended for use as an RF clipper, a limiting stage in IF amplifiers, or an RF Compressor in SSB transmitters. It contains a detector which may be used to detect AM but is particularly intended for use as an AGC detector. The amplifier, which has a gain of 12dB when not limiting, has upper and lower 3dB points of 150MHz and 5MHz respectively. It limits when its input exceeds 120mV rms. The detected output during limiting is 1mA.

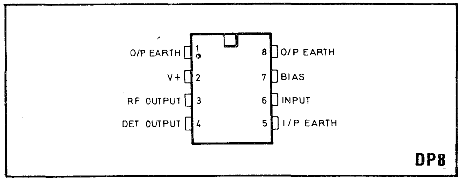


Fig. 1 Pin connections (top view)

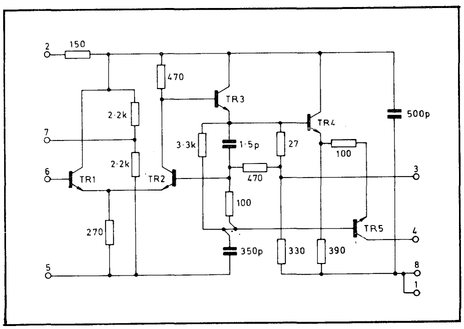


Fig. 2 Circuit diagram SL1613C

FEATURES

- Wide Bandwidth
- Low Noise
- Highly Symmetrical Limiting
- Large Signal Handling Capability

APPLICATIONS

- RF Clippers
- AGC Systems
- AM Detectors
- RF Compression in SSB Transmitters

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply +6V
Temperature +25°C
Pins 6 & 7 strapped together

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10	12	14	dB	30MHz
Upper 3dB frequency		150		MHz	
Lower 3dB frequency		5		MHz	
Noise figure		4.5		dB	60MHz 500Ω source
Supply current		15	20	mA	No signal
Limited RF o/p		1.25		V p-p	0.5V input, 30MHz
Detector current	0.8	1	1.3	mA	0.5V input, 30MHz
Maximum input before overload		1.75		V rms	30MHz
Input impedance		5kΩ// 6pF			60MHz Open circuit output

OPERATING NOTES

The SL1613C, like the SL1610/11/12, is normally used with the input and bias pins connected directly together and the input applied through a capacitor. However, and again like the SL1610/11/12, the bias may be decoupled and connected to the 'cold' end of a coil or tuned circuit, the input pin being connected to its 'hot' end or to a tap.

The supply rail is decoupled internally at RF but as the gain is dependent on supply voltage there should be no appreciable LF ripple on the supply. Two separate earth connections are made in order to minimise the effects of common earth-lead inductance – such common earth-lead inductance can cause instability and care should be taken not to introduce it externally.

The RF output is capable of driving a load of 1kΩ in parallel with 10pF. If a capacitive load of more than 10pF is envisaged a resistor should be connected between the output pin and the load. Normally 50Ω is sufficient. The output should be isolated at DC by a capacitor.

The detected output consists of a current out of pin 4, which is an NPN transistor collector. This pin must always be more than 3 volts more positive than earth, even if the detected output is not required (in which case it is best to strap pins 2 and 4).

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30°C to +85°C
Operating temperature	−30°C to +70°C
Supply voltage (pins 2 or 4)	+9V

PLESSEY
SEMICONDUCTORS

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1620C & SL1621C
AGC GENERATORS

The SL1621C is an AGC generator designed specifically for use in SSB receivers in conjunction with the SL1610C, SL1611C and SL1612C RF and IF amplifiers. In common with other advanced systems it generates a suitable AGC voltage directly from the detected audio waveform, provides a 'hold' period to maintain the AGC level during pauses in speech, and is immune to noise interference. In addition it will smoothly follow the fading signals characteristic of HF communication.

When used in a receiver comprising one SL1610C and one SL1612C amplifier and a suitable detector, the SL1621C will maintain the output within a 4dB range for a 110dB range of receiver input signal.

The SL1620C VOGAD (Voice Operated Gain Adjusting Device) is an AGC generator designed to work in conjunction with the SL1630C audio amplifier (particularly when the latter is used as a microphone amplifier) to maintain the amplifier output between 70mV and 87mV rms for a 35dB range of input. A one second 'hold' period is provided which prevents any increase of background noise during pauses in speech.

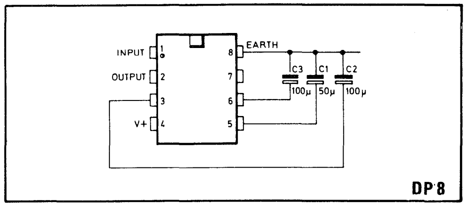


Fig. 1 Pin connections (top view)

FEATURES

- Wide Dynamic Range
- Speech Pause Memory
- Fast Attack/Adaptive Decay
- Only 4 External Components

APPLICATIONS

- Speech-Derived AGC Systems

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30 °C to +85° C
Supply voltage	−9V
Operating temperature	−30 °C to +70°C

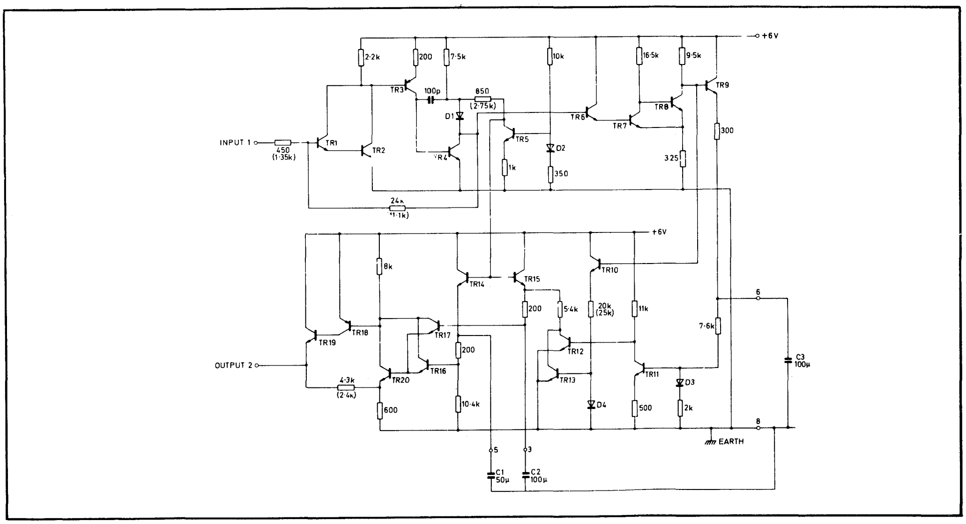


Fig. 2 Circuit diagram of SL1620C and SL1621C (component values for SL1620C are shown in brackets)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage = 6V
Temperature = +25°C
Input signal frequency = 1kHz

Characteristic	Circuit	Typical Value	Units	Test conditions	
Input for 0.65V DC output	SL1620C	70	mVrms	See Fig. 6	Measurement accuracy 1 dB
Input for 1.5V DC output	SL1620C	87	mVrms	See Fig. 6	
Input for 2.2V DC output	SL1621C	7.0	mVrms	See Fig. 7	
Input for 4.6V DC output	SL1621C	11.0	mVrms	See Fig. 7	
*Fast rise time, t_1	Both	20	ms	0–50% full output	C_1 = 50μF
*Fast decay time, t_2	Both	200	ms	100%–36% voltage on C_1	
*Slow rise time, t_3	Both	200	ms	Time to output transition point	C_2 = 100μF
Input 3 dB point	Both	10	kHz		
Maximum fade rate	SL1620C	0.22	V/s		
	SL1621C	0.45	V/s		
*Hold collapse time, t_4	Both	200	ms	Full-zero output	
*Hold time, t_5	Both	1.0	s	C_3 = 100μF	
AC ripple on output	Both	12	mVp-p	1kHz. Output open circuit	
Maximum output voltage	SL1620C	2	V		
	SL1621C	5	V		
Quiescent current consumption	Both	3	mA		
Surge current	Both	30	mA		
Input resistance	SL1620C	1.4	kΩ		
	SL1621C	500	Ω		
Output current	SL1620C	1.7	mA	@ + 2V output	
	SL1621C	2.5	mA	@ + 5.1V output	

*See Fig. 3

DESCRIPTION

The operation of the SL1621C is described with reference to the circuit diagram, Fig. 2 and Fig. 3 which illustrates the dynamic response of a receiver controlled by the SL1621C.

The SL1621C consists of an input AF amplifier TR1-TR4 (3dB point: 10KHz) coupled to a DC output amplifier, TR16-TR19, by means of a voltage back-off circuit, TR5 and two detectors, TR14 and TR15, having short and long rise and fall time constants respectively.

The detected audio signal at the input will rapidly establish an AGC level, via TR14, in time t_1 (see Fig. 3). Meanwhile the long time constant detector output will rise and after t_3 will control the output because this detector is the more sensitive.

If signals exist at the SL1621C input which are greater than approximately 4mV rms they will actuate the trigger circuit TR6-TR8 whose output pulses will provide a discharge current for C2 via TR10, TR13.

By this means the voltage on C2 can decay at a maximum rate, which corresponds to a rise in receiver gain of 20 dB/s. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However, should the receiver input signals fade faster than this, or disappear completely as during pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector will drop to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C3 via TR9, so holding off TR12 via TR11. When the trigger pulses cease, C3 discharges and after t_5 turns on TR12. Capacitor C2 is discharged rapidly (in time t_4) via TR12 and so full receiver gain is restored. The hold time, t_5 is approximately one second with C3 = 100µF. If signals reappear during t_5, then C3 will re-charge and normal operation will continue. The C3 re-charge time is made long enough to prevent prolongation of the hold time by noise pulses.

Fig. 3 shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

OPERATING NOTES

The various time constants quoted are for C1 = 50µF and C2 = C3 = 100µF. These time constants may be altered by varying the appropriate capacitors.

An input coupling capacitor is required. This should normally be 0.33µF for an SL1621C and about 1µF for an SL1620C.

Fig. 4 shows how the SL1621C may be connected into a typical SSB receiver.

Fig. 5 shows how the SL1620C is used to control the gain of the SL1630C audio amplifier. The operation of the SL1620C is exactly the same as that of the SL1621C and the diagram showing the dynamic response of the closed loop system, Fig. 3, is equally applicable to the SL1630C/SL1620C combination. Again, the time constants may be altered by varying the capacitor values.

The supply must either have a source resistance of less than 2Ω at LF or be decoupled by at least 500µF so that it is not affected by the current surge resulting from a sudden input on pin 1. The devices may be used with a supply of up to +9V.

In a receiver for both AM and SSB using an SL623C detector/carrier AGC generator, the AGC outputs of the SL1621C and SL623C may be connected together provided that no audio reaches the SL1621C input while the SL623C is controlling the system

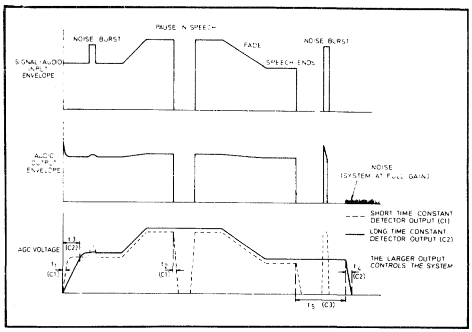


Fig. 3 Dynamic response

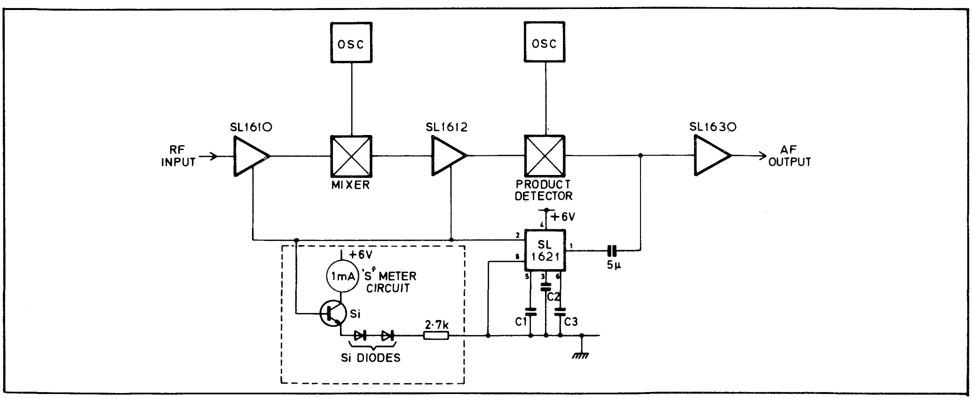


Fig. 4 SL1621C used to control an SSB receiver

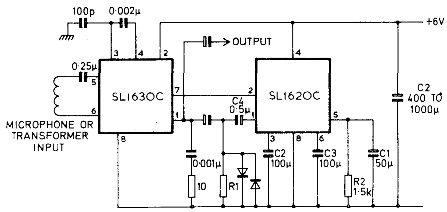


Fig. 5 SL1620C used to control an SL1630C audio amplifier

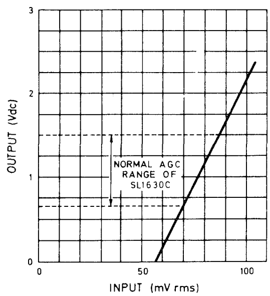


Fig. 6 Transfer characteristic of SL1620C

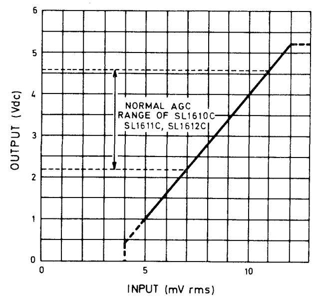


Fig. 7 Transfer characteristic of SL1621C

PLESSEY
SEMICONDUCTORS

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1623C

AM DETECTOR, AGC AMPLIFIER & SSB DEMODULATOR

The SL1623C is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator with SSB demodulator. It is designed specially for use in SSB/AM receivers in conjunction with SL1610C, SL1611C and SL1612C RF and IF amplifiers. It is complementary to the SL1621C SSB AGC generator.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL1610C and one SL1612C amplifier, the SL1623C will maintain the output within a 5 dB range for a 90 dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100 mV, contributes negligible distortion up to 90% modulation. The SSB demodulator is of single balanced form. The SL1623C is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies. The encapsulation is a 14 lead DIL package and the device is designed to operate from a 6 volt supply, over a temperature range of −30°C to +70°C.

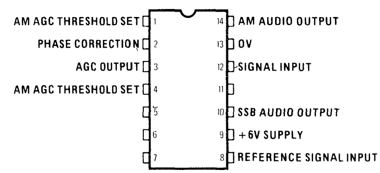


Fig. 1 Pin connection

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30°C to +85°C
Ambient operating temperature	0°C to +80°C
Supply voltage	−0.5V to +12V

ELECTRICAL CHARACTERISTICS @ SUPPLY = +6V, Tamb = +25°C

Characteristic	Value			Units	Test Conditions
	Min.	Typ.	Max.		
SSB Audio Output		30		mV rms	Signal Input 20mV rms @ 1.748 MHz. Ref. Signal Input 100mV rms @ 1.750 MHz
AM Audio Output		55		mV rms	Signal Input 125mV rms @ 1.75 MHz. Modulated to 80% @ 1kHz.
AGC Range (change in input level to increase AGC output voltage from 2.0V to 4.6V)		5		dB	Initial signal input 125mV rms at 1.75 MHz. Mod. to 80% at 1 kHz. Output Set with 10kΩ pot between pins 1&4 to 2.0V.
Quiescent Current Consumption		9		mA	Output open circuit.
Max. operating frequency		30		MHz	

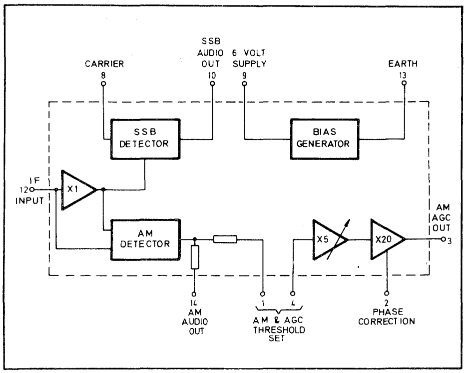


Fig. 2 Block Diagram

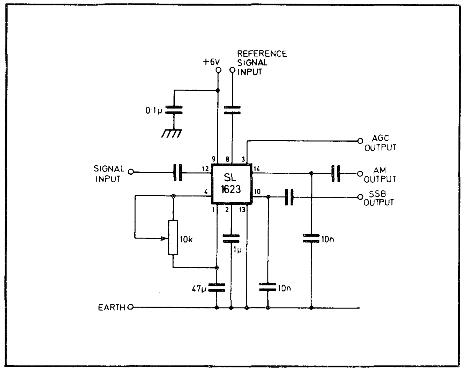


Fig. 3 Typical circuit using the SL1623C as signal detector and AGC

PLESSEY
SEMICONDUCTORS

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1625C
AM DETECTOR & AGC AMPLIFIER

The SL1625 is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator. It is designed specially for use in SSB/AM receivers in conjunction with SL1610C, SL1611C and SL1612C RF and IF amplifiers.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL1610C and SL1612C amplifier, the SL1625 will maintain the output within a 5 dB range for a 90 dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100 mV, contributes negligible distortion up to 90% modulation.

The SL1625 is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies. The encapsulation is an 8 lead DIL package and the device is designed to operate from a 6 volt supply, over a temperature range of 30°C to+70°C.

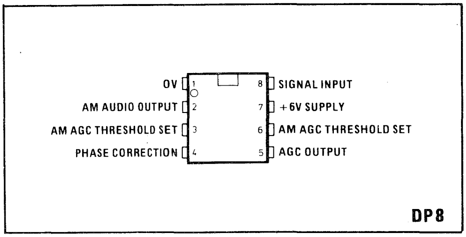


Fig. 1 Pin connection

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30°C to + 85°C
Supply voltage	−0.5V to +12V

ELECTRICAL CHARACTERISTICS @ SUPPLY =+6V, T_{amb} = +25°C

Characteristic	Value			Units	Test Conditions
	Min.	Typ.	Max.		
AM Audio Output	40	55	70	mV rms	Signal Input 125mV rms @ 1.75 MHz. Modulated to 80% @ 1 kHz.
AGC Range (change in input level to increase AGC output voltage from 2.0V to 4.6V)		5		dB	Initial signal input 125mV rms at 1.75 MHz. Mod. to 80% at 1 kHz. Output Set with 10k pot between pins 3 & 6 to 2.0V.
Quiescent Current Consumption		9	15	mA	Output open circuit.
Max. operating frequency		30		MHz	

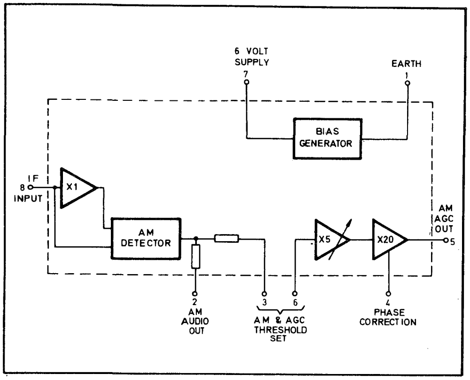


Fig. 2 Block Diagram

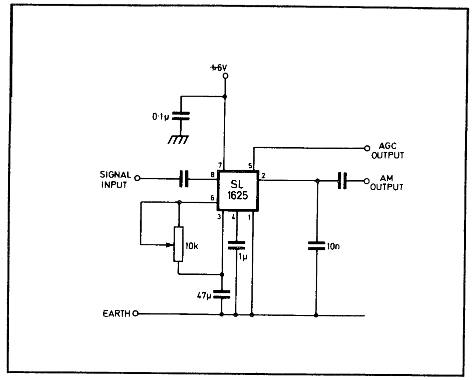


Fig. 3 Typical circuit using the SL1625 as signal detector and AGC generator.

PLESSEY
SEMICONDUCTORS

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1626C
AUDIO AMPLIFIER AND VOGAD

The SL1626C is a silicon integrated circuit combining the functions of audio amplifier with voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low-sensitivity microphone and to provide an essentially constant output signal for a 60dB range of input.

The encapsulation is an 8-lead plastic dual-in-line package and the device is designed to operate from a 6V ±0.5 volt supply, over a temperature range of -30°C to +70°C

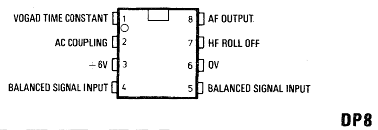


Fig. 1 Pin connections (top)

FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Prevention
- Speech Recording
- Level Setting Systems

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Input frequency 1kHz
Supply voltage +6V
Temperature +25°C

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
VOGAD output level	55	90	140	mV rms	Balanced signal input 18mV rms
AF amplifier voltage gain		52		dB	Balanced signal input 72uV rms
Quiescent current consumption		14	20	mA	6V supply
Decay time (see note 1)		1.0		s	Original balanced signal input 18mV rms
Attack time (see note 2)		20		ms	Original balanced signal input 1.8mV rms
Total harmonic distortion of VOGAD output		2		%	Balanced signal input 90mV rms
Differential input impedance		300		Ω	
Single-ended input impedance		180		Ω	
AF amplifier output resistance		50		Ω	
Minimum load resistance — AF amplifier o/p		1000		Ω	
VOGAD operating threshold (whisper threshold) at input		100		µV rms	
Input for 10% distortion		130		mV rms	
Supply line rejection at VOGAD o/p		15		dB	
Common mode signal handling		50		mV p-p	

NOTES

1. Decay time is the time for VOGAD output to return within 10% of original absolute level when signal input voltage is switched down 20dB.
2. Attack time is the time for VOGAD output to return to within 10% of original absolute level when signal input voltage is switched up 20dB.

OPERATING NOTES

The SL1626 will operate from a range of supply voltages from 4V up to 12V.

The input stage is a differential class A-B stage with AGC terminal. The accurate balance of the input stage and high common-mode rejection ratio of the second stage gives an overall common-mode rejection ratio of greater than 30dB.

Typically, the amplifier will handle differential input signals of up to 375mV p-p. When used in the unbalanced mode either pin 4 or pin 5 may be used as the input, the other being decoupled to earth.

The LF cut-off of the amplifier is set by C1 and also by the values of coupling capacitors to the input pins (pin 4 and pin 5). Coupling capacitors should be used if the DC potential of the input is not floating with respect to earth.

The HF cut-off is set by C2 (see Fig. 3). The VOGAD threshold may be increased by connecting and external conductance between pins 7 and 8. The threshold is increased by approximately 20dB for 1 millimho of conductance; the value of C2 should be adjusted in conjunction with any threshold alteration in order to obtain the desired bandwidth.

C3 and R1 set the attack and decay rates of the VOGAD. In Fig. 3, C3=47uF and R1=1Mohm which give an attack time constant (gain increasing) of 20ms and a decay rate of 20dB/s. C1=2.2uF and C2 =4.7nF give a 3dB bandwidth of approximately 300Hz to 3kHz.

ABSOLUTE MAXIMUM RATINGS

Continuous supply voltage (positive) 12V
Storage temperature −30°C to +85°C
Ambient operating temperature −30°C to +70°C

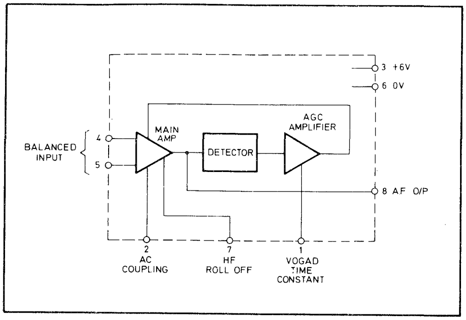


Fig. 2 Block diagram

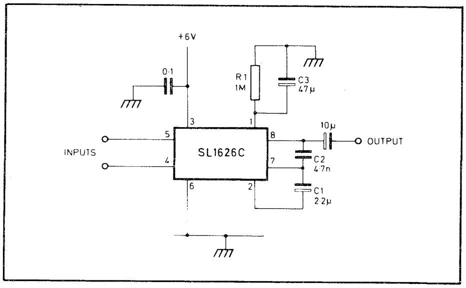


Fig. 3 Connection diagram for SL1626C used as a microphone amplifier

PLESSEY SEMICONDUCTORS

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1630C
MICROPHONE/HEADPHONE AMPLIFIER

The SL1630C is designed specifically for use as a microphone or headphone amplifier. It has a voltage gain of 100, will accept balanced or unbalanced inputs, and can deliver up to 200 mW output from a class AB push-pull output stage.

A gain control facility with a logarithmic law allows AGC to be applied when the device is used as a microphone amplifier, and also allows remote volume control with a linear potentiometer. Gain reduction of 60dB may be obtained.

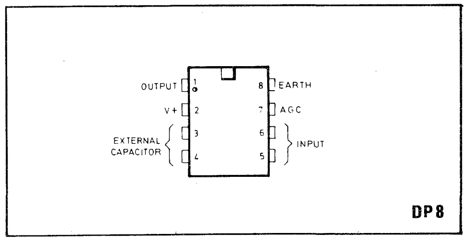


Fig. 1 Pin connections (top view)

FEATURES

- 40dB Gain
- Voltage-Controlled Gain
- 200 mW output
- Low Output Impedence

APPLICATIONS

- Low-Power Audio O/P Stages
- Preamplifiers (with or without AGC)

ABSOLUTE MAXIMUM RATINGS

Storage temperature		−30°C to + 85°C
Operating temperature		
	6V supply	−30°C to +70°C
	12V supply	−30°C to +70°C
Supply voltage		+15V

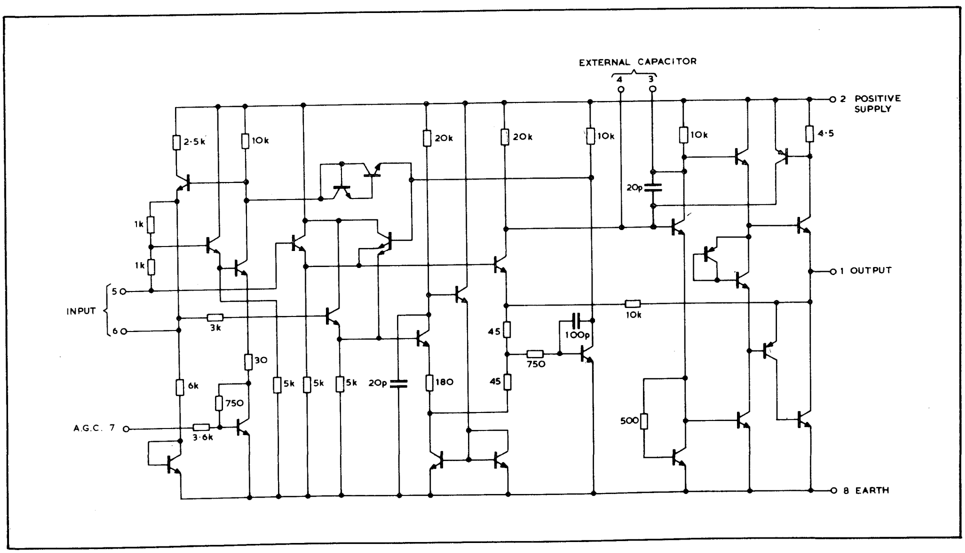


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature = +25°C
Signal Frequency = 1kHz
Supply = 12V

Characteristic	Typical Value	Units	Test conditions
Differential input voltage gain	40	dB	Input 1mVrms
Single ended input voltage gain	46	dB	Input 1mVrms
Maximum output voltage	1	Vrms	6V supply
	2	Vrms	12V supply
Maximum output power	See Fig. 7		0.5% distortion
Quiescent current (See also Fig. 7)	5	mA	6V supply
	12	mA	12V supply
Differential input impedance	2.0	kΩ	
Single ended input impedance	1.0	kΩ	
Output impedance	1.5	Ω	
Gain control range (See Fig. 6)	60	dB	
Maximum input (with gain reduced)	50	mVrms	10% distortion
Short circuit output current	110	mA	Irrespective of supply

OPERATING NOTES

Frequency Response

As with most small-signal integrated circuits, the inherent bandwidth of the SL1630C is quite large. It extends from low audio frequencies up to approximately 0.5 MHz, unless restricted by a roll-off capacitor (C1) connected between pins 3 and 4. The approximate upper cut-off frequency is then given by

$$\omega_C \simeq \frac{10^8}{C1}$$

Where C1 is in picofarads

Microphone Amplifier

Fig. 3 shows the SL1630C used with a balanced input on pins 5 and 6. If the load resistance increases with frequency it is necessary to stabilize the output circuitry. This is accomplished with 10Ω in series with 1nF connected between pin 1 and earth. The earth return to pin 8 must not share any common leads, particularly with the input. Decoupling pins 2 and 6 should follow normal engineering practice.

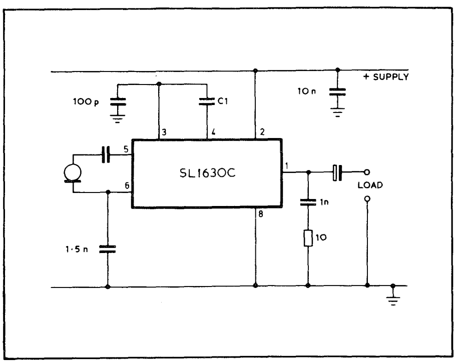


Fig. 3 SL1630C used as a microphone amplifier

Headphone Amplifier

Fig. 4 shows the SL1630C in a circuit suitable for powering a headset. The input is an unbalanced source connected to pin 5 and the device is decoupled at pins 1, 2 and 6 in the same manner as the microphone amplifier.

Manual gain adjustment using the remote gain control facility is also shown; R1 and R2 are chosen with regard to Fig. 6 to give the desired control range.

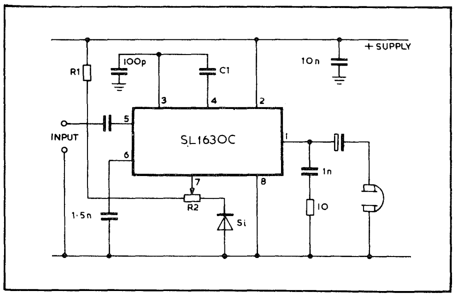


Fig. 4 SL1630C used as a headphone amplifier

Automatic Gain Control

To apply AGC, an SL1620C should be used as shown in the circuit of Fig. 5. This will give effective gain control with a low audio-frequency cut-off of 200 Hz and a control response time of approximately 20 ms.

To preserve low-frequency stability and prevent motor-boating, C4 should not exceed the value given and, whilst R1 should not exceed 300Ω, the time constant C3R1 must not be greater than 800 μs.

R2 is non-essential, but is useful if the input is likely to contain a large component below 300 Hz. C2 should be used if the power supply has a source impedance of more than a few ohms or is connected by long wires.

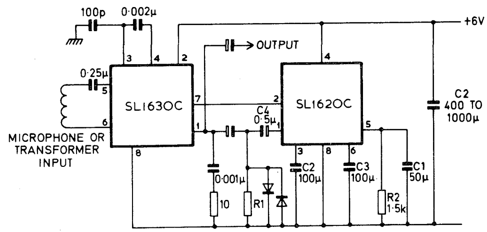


Fig. 5 SL1630C used with SL1620C to achieve automatic gain control

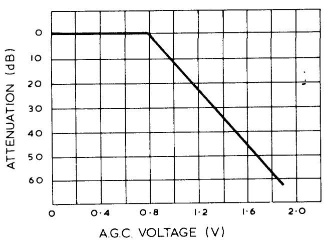


Fig. 6 AGC characteristics

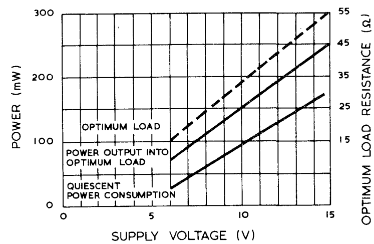


Fig. 7 Power characteristics

PLESSEY
SEMICONDUCTORS

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1640C & SL1641C

DOUBLE BALANCED MODULATORS

The SL1640C is designed to replace the conventional diode ring modulator, in RF and other communications systems, at frequencies of up to 75MHz. It offers a performance competitive with that of the diode ring while eliminating the associated transformers and heavy carrier drive power requirements.

At 30MHz, carrier and signal leaks are typically −40dB referred to the desired output product frequency. Intermodulation products are −45dB with a 60 mV rms input signal.

The SL1641C is a version of the SL1640C intended primarily for use in receiver mixer applications for which it offers a lower noise figure and lower power consumption. No output load resistor is included and signal leakage is higher, but otherwise the performance is identical to that of the SL1640C.

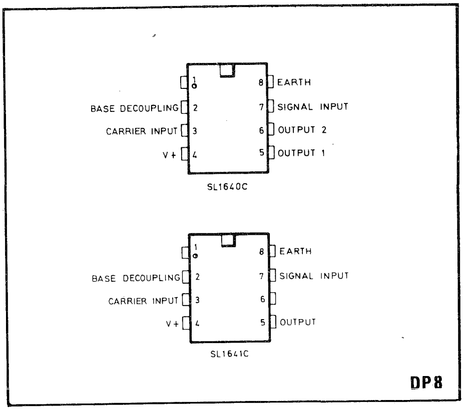


Fig. 1 Pin connections (top view)

FEATURES

- Low Carrier Leak
- Low Signal Leak
- Low Intermodulation Products
- Low Carrier Power Requirement
- Wide Bandwidth
- Minimal External Components

APPLICATIONS

- SSB and DSB Generators
- Detectors
- Phase Comparators
- Mixers

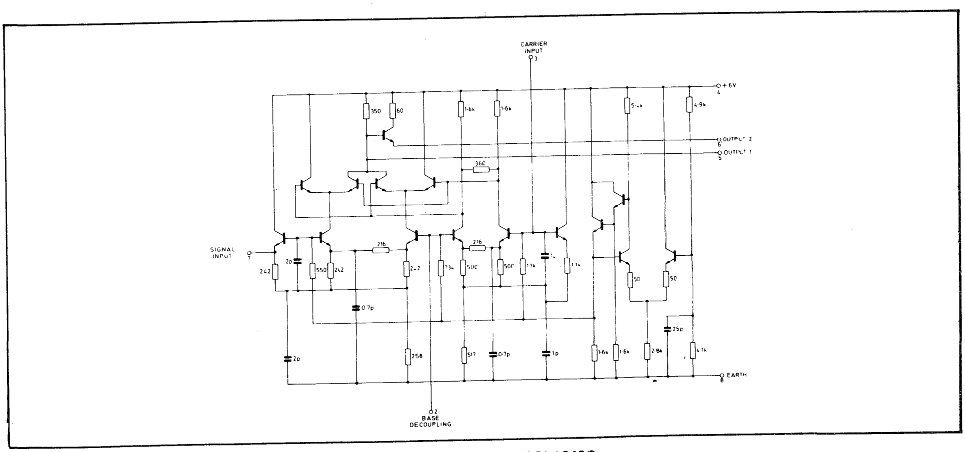


Fig. 2 Circuit diagram of SL1640C

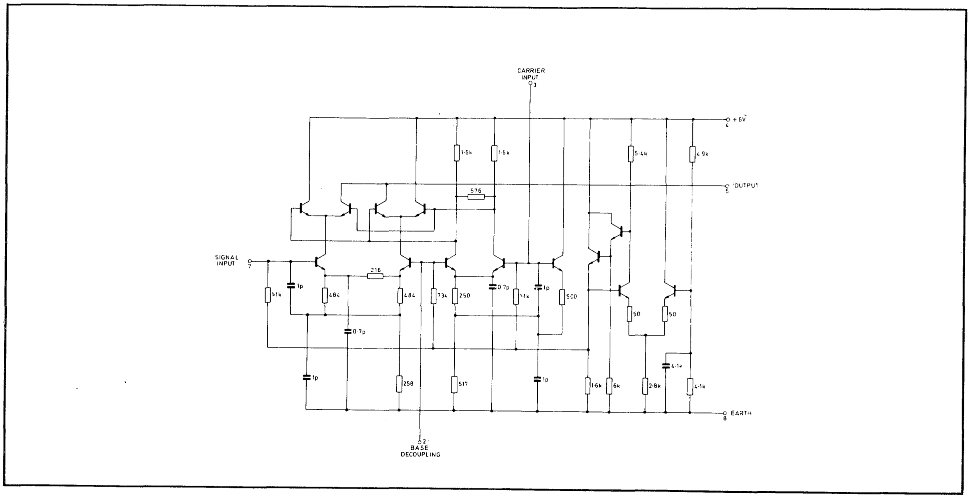


Fig. 3 Circuit diagram of SL1641C

OPERATING NOTES

The SL1640C circuit requires input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see electrical characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance.

Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at pin 2 would give rise to poor rejection figures and to distortion.

If the emitter follower is used, an external load resistor must be provided to supply emitter current. The quiescent output voltage from the emitter follower (pin 6) is +4.6V. To achieve maximum rejection figures at high frequencies, pin 1 (which is connected to the header) should be connected to earth and effective HT decoupling should be employed. The DC impedance should not exceed 800 ohms.

The SL1640C/1641C may be used with supply voltages of up to +9 volts with increased dissipation.

Signal and carrier leaks may be minimised with 10kΩ potentiometers and 330kΩ resistors connected as shown in Fig. 4. R1 is adjusted to minimise signal leak; R2 to minimise carrier leak.

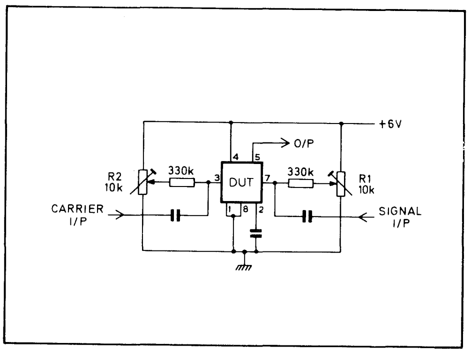


Fig. 4 Signal and carrier leak adjustments

The SL1641C is very similar to the SL1640C and similar operating notes apply. A current output is provided in the SL1641C to enable a tuned circuit to be directly connected. If both output sidebands are developed across the load (i.e. wideband operation), the AC impedance of the load must be less than 800Ω. If the output at one sideband frequency is negligible, the AC impedance may be raised to 1.6kΩ. It may be further raised if it is not desired to use the maximum input swing of 210mV rms. The DC resistance of the load should not exceed 800Ω.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage = +6V
Temperature = +25°C

Characteristics	Circuit	Typical Value	Units	Test conditions
Conversion gain	SL1640C	0	dB	
Signal leak [Signal output / Desired sideband output]	SL1640C	−40	dB	Signal: 70mVrms, 1.75MHz Carrier: 100mVrms, 28.25MHz Output: 30MHz
Carrier leak [Carrier output / Desired sideband output]	SL1640C	−40	dB	
Intermodulation products	SL1640C	−45	dB	Signal 1: 42.5mVrms, 1.75MHz Signal 2: 42.5mVrms, 2MHz Carrier: 100mVrms, 28.25MHz Output: 29.75MHz
Conversion gain	SL1641C	0	dB	400Ω load Signal: 70mVrms, 30MHz
Signal leak	SL1641C	−18	dB	Carrier: 100mVrms, 28.25MHz Output: 1.75MHz
Carrier leak	SL1641C	−25	dB	
Intermodulation products	SL1641C	−45	dB	Signal 1: 42.5mVrms, 30MHz Signal 2: 42.5mVrms, 31MHz Carrier: 100mVrms, 28.25MHz Output: 3.75MHz
Carrier input impedance	Both	1kΩ//4pF		
Signal input impedance	SL1640C	500Ω//5pF		
	SL1641C	1kΩ//4pF		
Output impedance	SL1640C	350Ω//8pF		Output 1
(see Operating Notes)	SL1641C	8pF		
Max. input before limiting	SL1640C	210	mVrms	
	SL1641C	250	mVrms	
Quiescent current consumption	SL1640C	12	mA	
	SL1641C	10	mA	
Noise figure	SL1640C	15	dB	
	SL1641C	12	dB	
Signal leak variation	Both	±2	dB	
Carrier leak variation	Both	±2	dB	
Conversion gain variation with temperature	Both	±1	dB	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

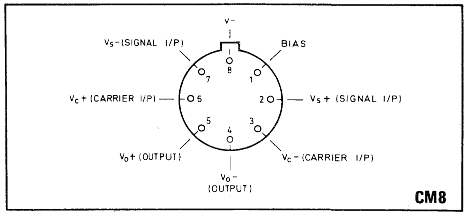
Storage temperature	−55°C to +175°C
Operating temperature	0°C to +70°C
Supply voltage	+9V

PLESSEY
SEMICONDUCTORS

SL1696C

DOUBLE-BALANCED MODULATOR/DEMODULATOR

The SL1696 is a versatile monolithic integrated circuit double balanced modulator/demodulator, designed for use where the output voltage is the product of the signal input voltage and the switching carrier voltage. The SL1696 has an operating temperature range of 0°C to +70°C.



FEATURES

- Carrier Suppression 65dB Typ. @500 kHz; 50dB Typ. @ 10 MHz
- Common Mode Rejection 85dB Typ.
- Gain and Signal Handling Both Adjustable
- Balanced Inputs and Outputs

APPLICATIONS

- DSB, DSBSC, AM Modulation
- Synchronous Detection
- FM Detection
- Phase Detection
- Chopper and Signal Routeing Applications

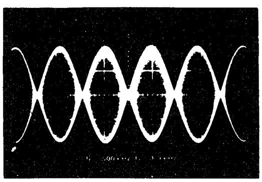


Fig. 1 Suppressed carrier output waveform

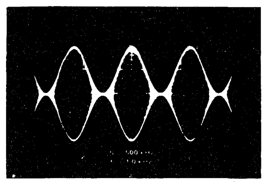


Fig. 2 AM output waveform

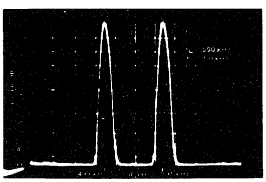


Fig. 3 Suppressed carrier spectrum

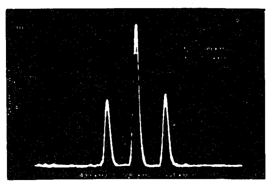


Fig. 4 AM spectrum

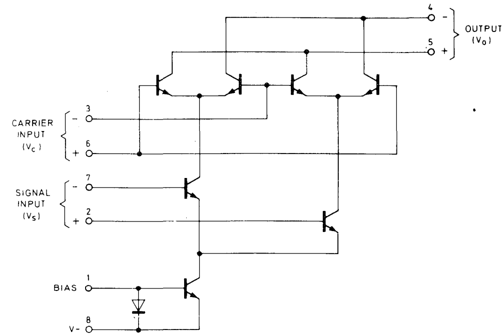


Fig. 5 Circuit diagram

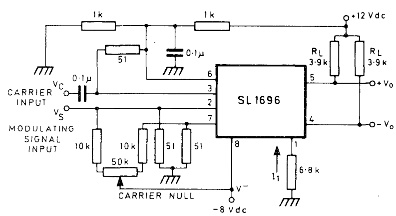


Fig. 6 Typical modulator circuit

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise stated

Rating	Symbol	Value	Units
Applied Voltage ($V_5 - V_6$, $V_3 - V_2$, $V_4 - V_6$, $V_4 - V_3$, $V_6 - V_7$, $V_6 - V_2$, $V_3 - V_7$, $V_5 - V_3$)	ΔV	20	VDC
Differential Input Signal	$V_6 - V_3$	+5.0	VDC
	$V_7 - V_2$	± 5	VDC
Maximum Bias Current	I_1	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		575	mW
Derate above T_A = +25°		3.85	mW/°C
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
V^+ = +12V DC, V^- = −8V DC, I_1 = 1.0 mA DC, R_L = 3.9 kΩ, T_A = +25°C
All input and output characteristics single-ended, unless otherwise stated.

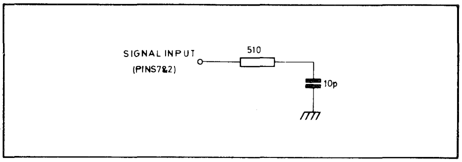
Characteristic	Fig.	Note	Symbol	Value Min.	Value Typ.	Value Max.	Units
Carrier Feedthrough	7	1	V_{CFT}				μV(rms)
V_C = 60 mV(rms) sinewave and f_C = 1.0 kHz				–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	
V_C = 300 mVp-p square wave							mV(rms)
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	200	
Carrier Suppression	7	2	V_{CS}				dB
f_S = 10 kHz, 300 mV(rms)							
f_C = 500 kHz, 60 mV(rms) sinewave				40	65	–	
f_C = 10 MHz, 60 mV(rms) sinewave				–	50	–	
Transadmittance Bandwidth (R_L = 50 ohms)	10	8	BW_{3dB}				MHz
Carrier Input Port, V_C = 60 mV(rms) sinewave				–	300	–	
f_S = 1.0 kHz, 300 mV(rms) sinewave							
Signal Input Port, V_S = 300 mV(rms) sinewave				–	80	–	
V_C = 0.5 V DC							
Signal Gain	12	3	A_{VS}	2.5	3.5	–	V/V
V_S = 100 mV(rms), f = 1.0 kHz; V_C = 0.5 V DC							
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	8	–					
Parellel Input Resistance			r_{ip}	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz	8	–					
Parallel Output Resistance			r_{op}	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	pF
Input Bias Current	9	–					μA
$I_{bS} = \frac{I_2 + I_7}{2}$; $I_{bC} = \frac{I_6 + I_3}{2}$			I_{bS}	–	12	30	
			I_{bC}	–	12	30	
Input Offset Current	9	–					μA
$I_{ioS} = I_2 - I_7$; $I_{ioC} = I_6 - I_3$			I_{ioS}	–	0.7	7.0	
			I_{ioC}	–	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	9	–	TC_{Iio}	–	2.0	–	nA/°C
Output Offset Current ($I_5 - I_4$)	9	–	I_{oo}	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	9	–	TC_{Ioo}		90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	11	4	CMV	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C \rvert$ = 0.5 V DC	11	–	A_{CM}	–	−85	–	dB
Common-Mode Quiescent Output Voltage (Pin 5 or Pin 4)	12	–	V_o	–	8.0	–	V DC
Differential Output Voltage Swing Capability	12	–	V_{out}	–	8.0	–	Vp-p
Power Supply Current	9	6					mA DC
$I_5 + I_4$			I_D^+	–	1.0	2.0	
I_8			I_D^-	–	2.0	3.0	
DC Power Dissipation	9	5	P_D	–	33	–	mW

Note 10 – Output Signal, V_o

The output signal is taken from pins 5 and 4, either balanced or single-ended.

Note 11 – Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternative method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 2 and 7. In this case input current drift may cause serious degradation of carrier suppression.

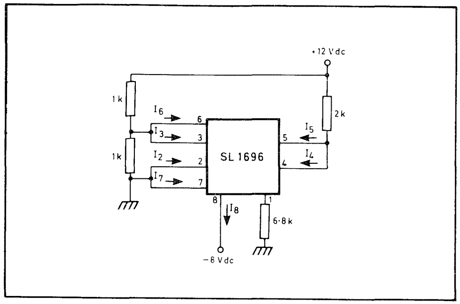


Fig. 9 Bias and offset currents

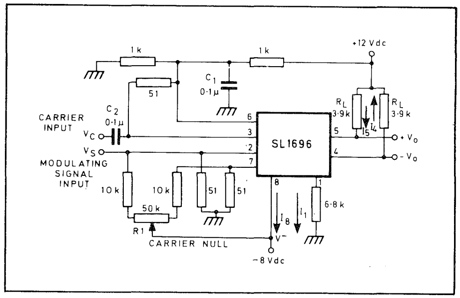


Fig. 10 Transconductance bandwidth

TEST CIRCUITS (FIGS. 7 TO 12)

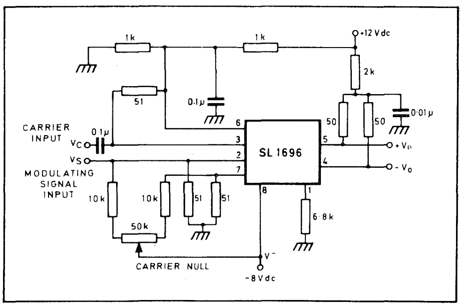


Fig. 7 Carrier rejection and suppression

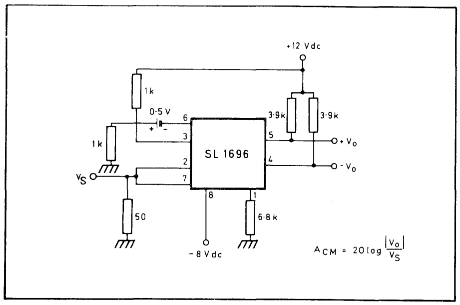


Fig. 11 Common-mode gain

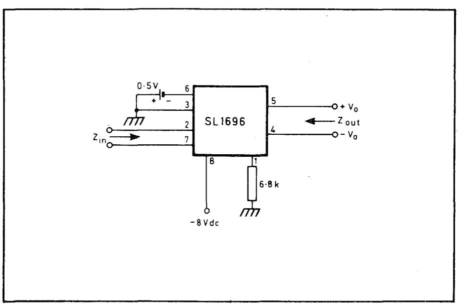


Fig. 8 Input/output impedance

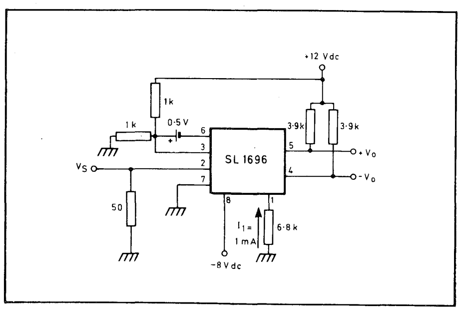


Fig. 12 Signal gain and output swing

OPERATING NOTES

Note 1 – Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Fig. 7).

Note 2 – Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The SL1696 has been characterized with a 60 mV(rms) sinewave carrier input signal.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 – Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{2r_e}$$

$$r_e = \frac{26\text{mV}}{I_1\ (\text{mA})}$$

A constant DC potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 V). This in effect forms a cascode differential amplifier.

Note 4 – Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 – Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_4 = V_5$, $I_1 = I_5 = I_4$ and ignoring base current, $P_D = 2I_1(V_5 - V_8) + I_1(V_1 - V_8)$ where subscripts refer to TO-5 package pin numbers.

Note 6 – Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at pin 1 Assume:

$$I_4 = I_5 = I_1$$
$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_1 = \frac{V^- - \theta}{I_1} - 500\Omega$$

where: R_1 is the resistor between pin 1 and ground

$\theta = 0.75$ V at $T_A = +25°C$

The SL1696 has been characterized for the condition I = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_4 = V_5 = V^+ - I_1 R_L$$

Note 7 – Biasing

The SL1696 requires three DC bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$20\text{V} \geq [(V_5\ V_4) - (V_6\ V_3)] \geq 2\text{V}$$
$$20\text{V} \geq [(V_6\ V_3) - (V_2\ V_7)] \geq 2.7\text{V}$$
$$20\text{V} \geq [(V_2\ V_7) - (V_1)] \geq 2.7\text{V}$$

The foregoing conditions are based on the following approximations:

$$V_5 = V_4 \qquad V_6 = V_3 \qquad V_2 = V_7$$

Bias currents flowing into pins 2, 7, 6 and 3 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 – Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21C} = \frac{i_o\ (\text{each sideband})}{V_S\ (\text{signal})}\bigg|\ V_o = 0$$

Signal transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21S} = \frac{i_o\ (\text{signal})}{V_S\ (\text{signal})}\bigg|\ V_C = 0.5\text{ Vdc}, V_o = 0$$

Note 9 – Coupling and Bypass Capacitors C_1 and C_2

Capacitors C_1 and C_2 (Fig. 7) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

OPERATING PRINCIPLES

The SL1696, a monolithic balanced modulator circuit, is shown in Fig. 5.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with a current source. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant multiplied by the product of the two input signals.

Mathematical analysis of linear AC signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, double balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristcs.

External load resistors are employed at the device output.

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant time the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier and lower differential amp has its emitters internally connected, this voltage applies to the input ports for all conditions.

The gain from the modulating signal input port to the output is the SL1696 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the SL1696 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level DC
2) High-level DC
3) Low-level AC
4) High-level AC

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level DC	$\dfrac{R_L V_C}{4r_e \frac{KT}{q}}$	f_M
High-level DC	$\dfrac{R_L}{2r_e}$	f_M
Low-level AC	$\dfrac{R_L V_C(rms)}{2\sqrt{2}\frac{KT}{q} 2r_e}$	$f_C \pm f_M$
High-level AC	$\dfrac{0.637 R_L}{2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$ $5f_C \pm f_M, \ldots$

Table 1 Voltage gain and output frequencies

NOTES:

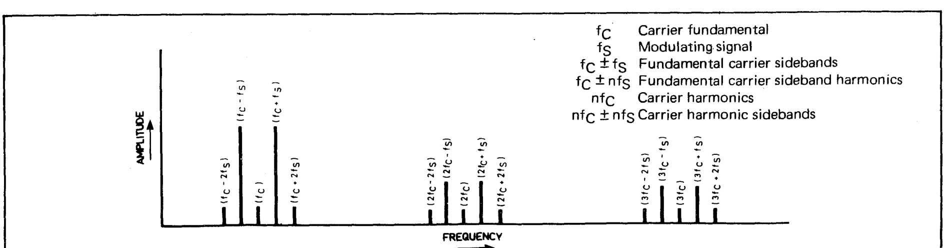
1. Low-level Modulating Signal, V_M assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. r_e = Transistor dynamic emitter resistance, At +25°C;

$$r_e \approx \frac{26\text{ mV}}{I_s\text{ (mA)}}$$

6. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26\text{ mV at room temperature}$$

DEFINITIONS



APPLICATION NOTES

Double sideband suppressed carrier modulation is the basic application of the SL1696. The suggested circuit for this application is shown in Fig. 6, on page 2 of this data sheet.

In some applications, it may be necessary to operate the SL1696 with a single DC supply voltage instead of dual supplies. Fig. 13 shows a balanced modulator designed for operation with a single +12V supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Fig. 14 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Fig. 14 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Fig. 15.

Product Detector

The SL1696 makes an excellent SSB product detector (see Fig. 16).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1μF capacitors on pins 6 and 3 should be increased to 1.0μF. Also, the output filter at pin 4 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

Double Balanced Mixer

The SL1696 may be used as a double balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Fig. 17 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The SL1696 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figs. 18 and 19 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The SL1696 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the SL1696 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The SL1696 will then provide an output which is a function of the input signal frequency,

TYPICAL APPLICATIONS (FIGS. 13 TO 19)

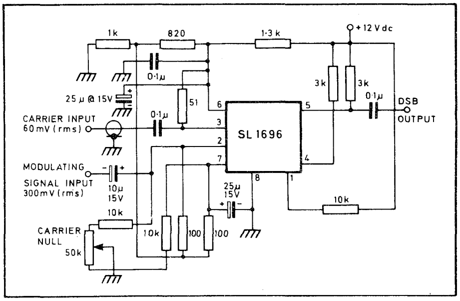


Fig. 13 Balanced modulator (+12V single supply)

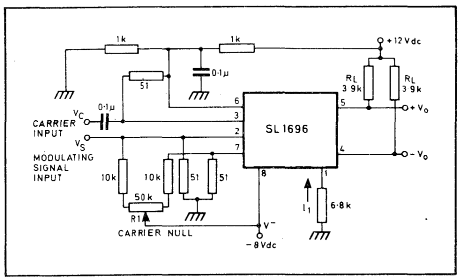


Fig. 14 Balanced modulator/demodulator

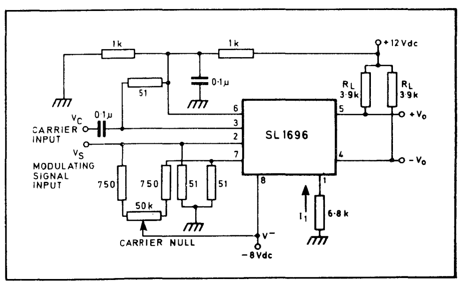


Fig. 15 AM modulator

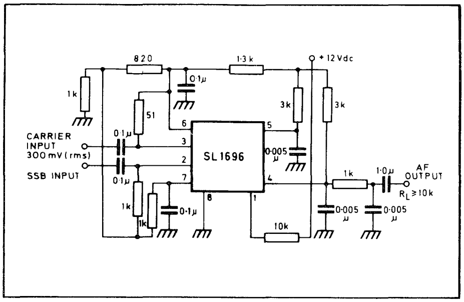


Fig. 16 Product detector (+12V single supply)

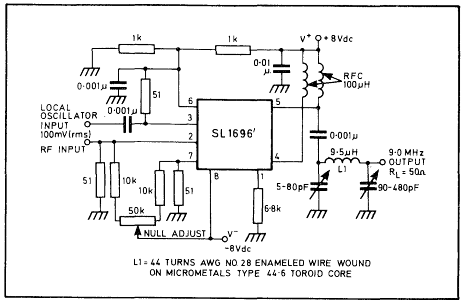


Fig. 17 Double-balanced mixer (broadband inputs, 9.0 MHz tuned output)

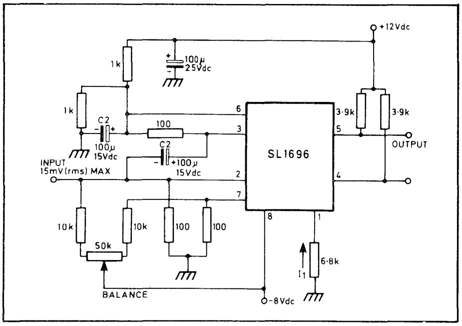


Fig. 18 Low frequency doubler

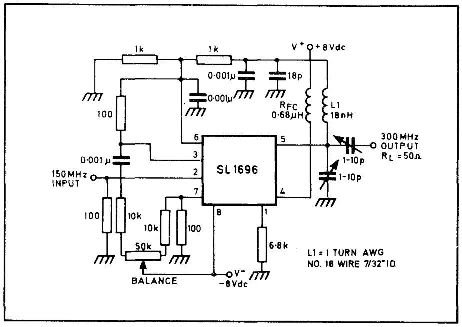


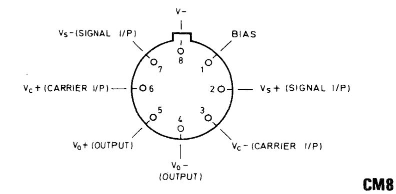
Fig. 19 150 to 300 MHz doubler

PLESSEY
SEMICONDUCTORS

SL1796C

DOUBLE-BALANCED MODULATOR/DEMODULATOR

The SL1796 is a versatile monolithic integrated circuit double balanced modulator/demodulator, designed for use where the output voltage is the product of the signal input voltage and the switching carrier voltage. The SL1796 has an operating temperature range of 0°C to +70°C.



FEATURES

- Carrier Suppression 65dB Typ. @500 kHz; 50dB Typ. @10 MHz
- Common Mode Rejection 85dB Typ.
- Gain and Signal Handling Both Adjustable
- Balanced Inputs and Outputs

APPLICATIONS

- DSB, DSBSC, AM Modulation
- Synchronous Detection
- FM Detection
- Phase Detection
- Chopper and Signal Routeing Applications

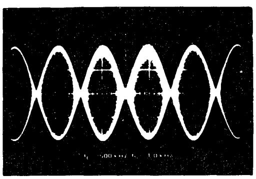


Fig. 1 Suppressed carrier output waveform

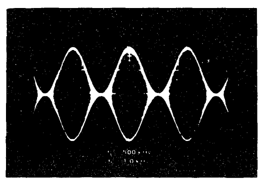


Fig. 2 AM output waveform

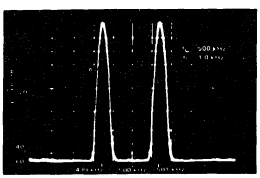


Fig. 3 Suppressed carrier spectrum

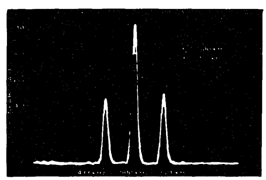


Fig. 4 AM spectrum

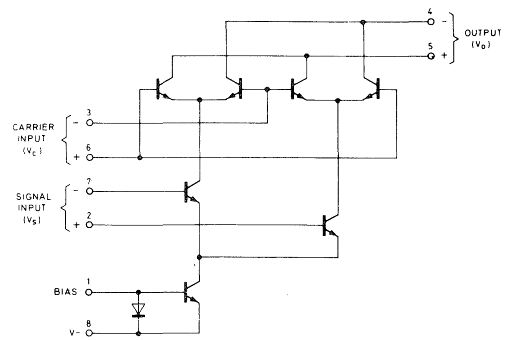


Fig. 5 Circuit diagram

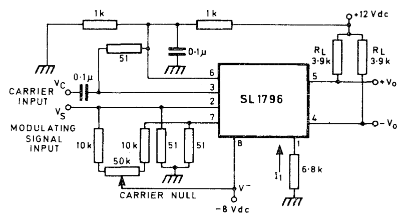


Fig. 6 Typical modulator circuit

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise stated

Rating	Symbol	Value	Units
Applied Voltage ($V_5 - V_6$, $V_3 - V_2$, $V_4 - V_6$, $V_4 - V_3$, $V_6 - V_7$, $V_6 - V_2$, $V_3 - V_7$, $V_5 - V_3$)	ΔV	45	VDC
Differential Input Signal	$V_6 - V_3$ $V_7 - V_2$	+5.0 ± 5	VDC VDC
Maximum Bias Current	I_1	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		575	mW
Derate above T_A = +25°		3.85	mW/°C
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

$V^+ = +12V$ DC, $V^- = -8V$ DC, $I_1 = 1.0$ mA DC, $R_L = 3.9\ k\Omega$, $T_A = +25°C$

All input and output characteristics single-ended, unless otherwise stated.

Characteristic	Fig.	Note	Symbol	Value			Units
				Min.	Typ.	Max.	
Carrier Feedthrough	7	1	V_{CFT}				μV(rms)
V_C = 60 mV(rms) sinewave and f_C = 1.0 kHz				–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	
V_C = 300 mVp-p square wave							mV(rms)
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	200	
Carrier Suppression	7	2	V_{CS}				dB
f_S = 10 kHz, 300 mV(rms)							
f_C = 500 kHz, 60 mV(rms) sinewave				40	65	–	
f_C = 10 MHz, 60 mV(rms) sinewave				–	50	–	
Transadmittance Bandwidth (R_L = 50 ohms)	10	8	BW_{3dB}				MHz
Carrier Input Port, V_C = 60 mV(rms) sinewave				–	300	–	
f_S = 1.0 kHz, 300 mV(rms) sinewave							
Signal Input Port, V_S = 300 mV(rms) sinewave				–	80	–	
V_C = 0.5 V DC							
Signal Gain	12	3	A_{VS}	2.5	3.5	–	V/V
V_S = 100 mV(rms), f = 1.0 kHz; V_C = 0.5 V DC							
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	8	–					
Parellel Input Resistance			r_{ip}	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz	8	–					
Parallel Output Resistance			r_{op}	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	pF
Input Bias Current	9	–					μA
$I_{bS} = \frac{I_2 + I_7}{2}$; $I_{bC} = \frac{I_6 + I_3}{2}$			I_{bS}	–	12	30	
			I_{bC}	–	12	30	
Input Offset Current	9	–					μA
$I_{ioS} = I_2 - I_7$; $I_{ioC} = I_6 - I_3$			$\|I_{ioS}\|$	–	0.7	7.0	
			$\|I_{ioC}\|$	–	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = –55°C to +125°C)	9	–	$\|TC_{Iio}\|$	–	2.0	–	nA/°C
Output Offset Current ($I_5 - I_4$)	9	–	$\|I_{oo}\|$	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = –55°C to +125°C)	9	–	$\|TC_{Ioo}\|$		90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	11	4	CMV	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\|V_C\|$ = 0.5 V DC	11	–	A_{CM}	–	–85	–	dB
Common-Mode Quiescent Output Voltage (Pin 5 or Pin 4)	12	–	V_o	–	8.0	–	V DC
Differential Output Voltage Swing Capability	12	–	V_{out}	–	8.0	–	Vp-p
Power Supply Current	9	6					mA DC
$I_5 + I_4$			I_D^+	–	2.0	4.0	
I_8			I_D^-	–	3.0	5.0	
DC Power Dissipation	9	5	P_D	–	33	–	mW

Note 1 — Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Fig. 7).

Note 2 — Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The SL1796 has been characterized with a 60 mV(rms) sinewave carrier input signal.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair — or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 — Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_O}{V_S} = \frac{R_L}{2r_e}$$

$$r_e = \frac{26\text{mV}}{I_1\ (\text{mA})}$$

A constant DC potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 V). This in effect forms a cascode differential amplifier.

Note 4 — Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 — Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_4 = V_5$, $I_1 = I_5 = I_4$ and ignoring base current, $P_D = 2I_1 (V_5 - V_8) + I_1 (V_1 - V_8)$ where subscripts refer to TO-5 package pin numbers.

Note 6 — Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at pin 1 Assume:

$$I_4 = I_5 = I_1$$
$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_1 = \frac{V^- - \theta}{I_1} - 500\Omega$$

where: R_1 is the resistor between pin 1 and ground

θ = 0.75 V at T_A = +25°C

The SL1796 has been characterized for the condition I = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_4 = V_5 = V^+ - I_1 R_L$$

Note 7 — Biasing

The SL1796 requires three DC bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$20V \geqslant [(V_5\ V_4) - (V_6\ V_3)] \geqslant 2V$$
$$20V \geqslant [(V_6\ V_3) - (V_2\ V_7)] \geqslant 2.7V$$
$$20V \geqslant [(V_2\ V_7) - (V_1)] \geqslant 2.7V$$

The foregoing conditions are based on the following approximations:

$$V_5 = V_4 \qquad V_6 = V_3 \qquad V_2 = V_7$$

Bias currents flowing into pins 2, 7, 6 and 3 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 — Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21C} = \frac{i_o\ (\text{each sideband})}{V_S\ (\text{signal})} \bigg|\, V_o = 0$$

Signal transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21S} = \frac{i_o'\ (\text{signal})}{V_S\ (\text{signal})} \bigg|\, V_C = 0.5\ \text{Vdc}, V_o = 0$$

Note 9 — Coupling and Bypass Capacitors C_1 and C_2

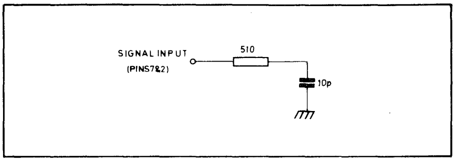
Capacitors C_1 and C_2 (Fig. 7) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Note 10 – Output Signal, V_o

The output signal is taken from pins 5 and 4, either balanced or single-ended.

Note 11 – Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternative method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 2 and 7. In this case input current drift may cause serious degradation of carrier suppression.

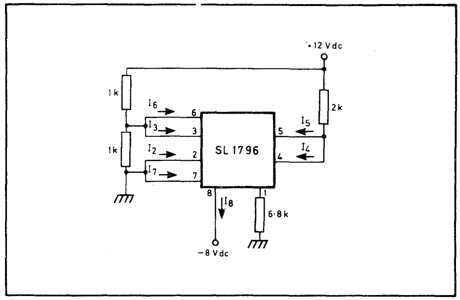


Fig. 9 Bias and offset currents

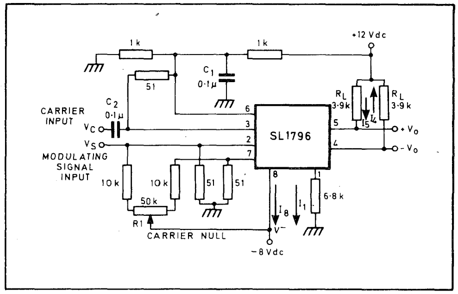


Fig. 10 Transconductance bandwidth

TEST CIRCUITS (FIGS. 7 TO 12)

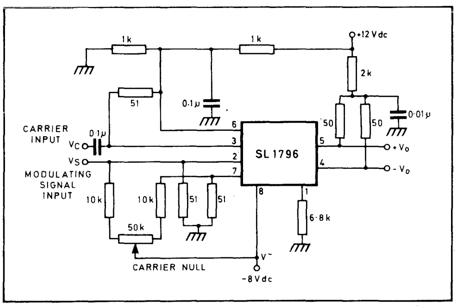


Fig. 7 Carrier rejection and suppression

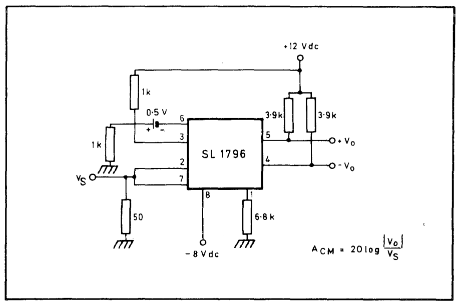


Fig. 11 Common-mode gain

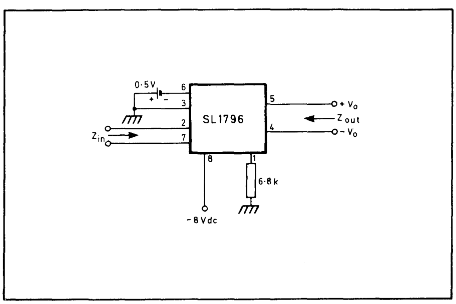


Fig. 8 Input/output impedance

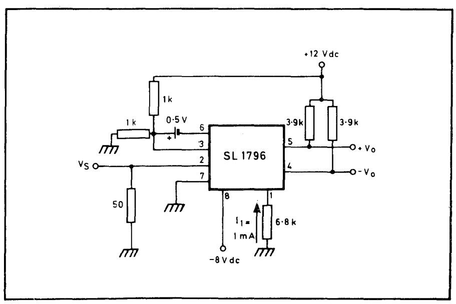


Fig. 12 Signal gain and output swing

OPERATING PRINCIPLES

The SL1796, a monolithic balanced modulator circuit, is shown in Fig. 5.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with a current source. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant multiplied by the product of the two input signals.

Mathematical analysis of linear AC signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, double balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristcs.

External load resistors are employed at the device output.

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant time the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier and lower differential amp has its emitters internally connected, this voltage applies to the input ports for all conditions.

The gain from the modulating signal input port to the output is the SL1796 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the SL1796 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level DC
2) High-level DC
3) Low-level AC
4) High-level AC

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level DC	$\dfrac{R_L V_C}{4r_e \frac{KT}{q}}$	f_M
High-level DC	$\dfrac{R_L}{2r_e}$	f_M
Low-level AC	$\dfrac{R_L\ V_C(rms)}{2\sqrt{2}\frac{KT}{q}\ 2r_e}$	$f_C \pm f_M$
High-level AC	$\dfrac{0.637\ R_L}{2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$ $5f_C \pm f_M, \ldots$

Table 1 Voltage gain and output frequencies

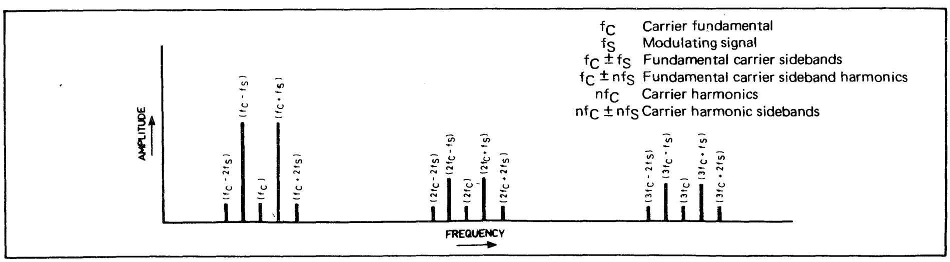
NOTES:
1. Low-level Modulating Signal, V_M assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. r_e = Transistor dynamic emitter resistance, At +25°C;

$$r_e \approx \frac{26\ \text{mV}}{I_s\ (\text{mA})}$$

6. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26\ \text{mV at room temperature}$$

DEFINITIONS



APPLICATION NOTES

Double sideband suppressed carrier modulation is the basic application of the SL1796. The suggested circuit for this application is shown in Fig. 6, on page 2 of this data sheet.

In some applications, it may be necessary to operate the SL1796 with a single DC supply voltage instead of dual supplies. Fig. 13 shows a balanced modulator designed for operation with a single +12V supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Fig. 14 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Fig. 14 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Fig. 15.

Product Detector

The SL1796 makes an excellent SSB product detector (see Fig. 16).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1μF capacitors on pins 6 and 3 should be increased to 1.0μF. Also, the output filter at pin 4 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

Double Balanced Mixer

The SL1796 may be used as a double balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Fig. 17 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The SL1796 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figs. 18 and 19 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The SL1796 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the SL1796 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The SL1796 will then provide an output which is a function of the input signal frequency,

TYPICAL APPLICATIONS (FIGS. 13 TO 19)

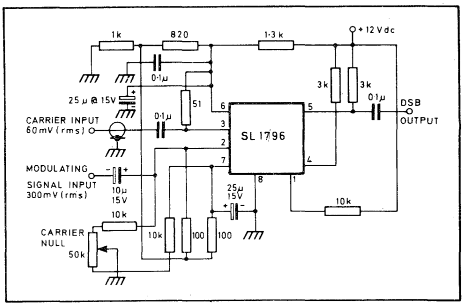


Fig. 13 Balanced modulator (+12V single supply)

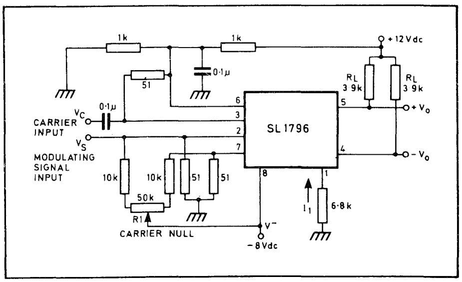


Fig. 14 Balanced modulator/demodulator

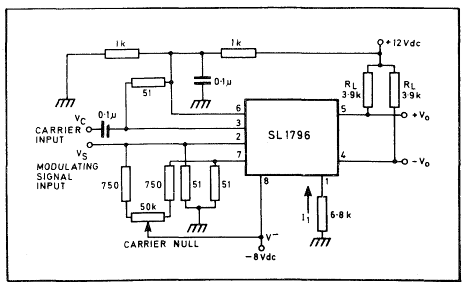


Fig. 15 AM modulator

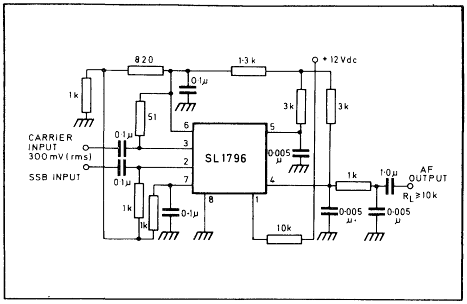


Fig. 16 Product detector (+12V single supply)

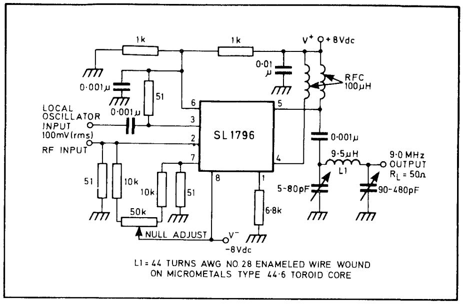


Fig. 17 Double-balanced mixer (broadband inputs, 9.0 MHz tuned output)

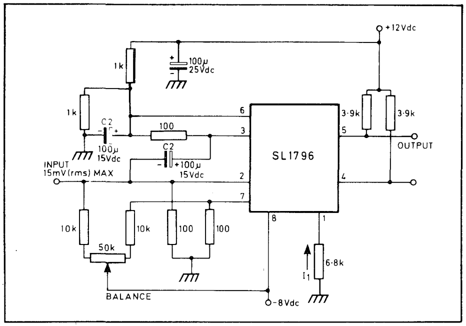


Fig. 18 Low frequency doubler

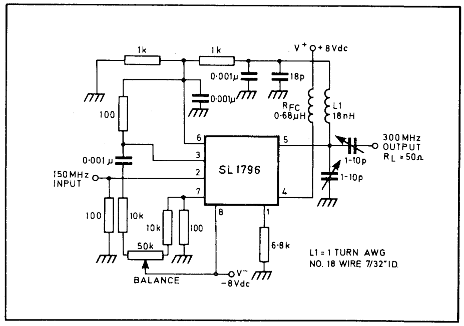


Fig. 19 150 to 300 MHz doubler

PLESSEY
SEMICONDUCTORS

SL3000 SERIES
TRANSISTOR ARRAYS

SL3045C SL3046C
TRANSISTOR ARRAYS

The SL3045 and SL3046 are monolithic arrays of five general purpose high frequency transistors arranged as a differential pair and three isolated transistors. The transistors feature a V_{BE} matching of, typically, better than $\pm$ 5mV between any pair, an f_T of 300MHz and a low noise figure.

The SL3045 is available only in a ceramic dual-in-line package; the SL3046 is packaged in plastic dual-in-line.

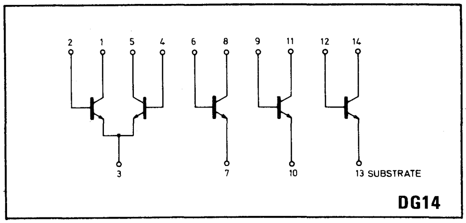


Fig. 1 Pin connections

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = +25°C

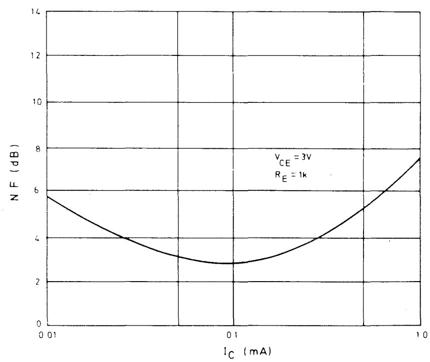
Static Characteristics

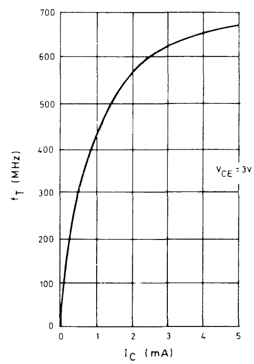
Symbol	Characteristic	Value Min.	Value Typ.	Value Max.	Units	Test conditions
BV_{EBO}	Emitter-base breakdown	5			V	I_E = 10μA
BV_{CEO}	Collector-emitter breakdown	15			V	I_C = 1mA
BV_{CBO}	Collector-base breakdown	20	50		V	I_C = 10μA
BV_{CIO}	Collector-substrate breakdown	20	70		V	I_C = 10μA
I_{CEO}	Collector cut off current			0.5	μA	V_{CE} = 10V, I_B = 0
I_{CBO}	Collector cut off current			4	nA	V_{CB} = 10V, I_E = 0
$V_{BE(ON)}$	Base emitter voltage		0.71		V	V_{CE} = 3V I_C = 1mA
			0.78		V	V_{CE} = 3V I_C = 10mA
$V_{CE(SAT)}$	Collector-emitter saturation		0.3		V	I_B = 1mA I_C = 10mA
h_{FE}	Static forward current-transfer		120			V_{CE} = 3V I_C = 10mA
	ratio	40	100			V_{CE} = 3V I_C = 1mA
			50			V_{CE} = 3V I_C = 10μA
I_{IO}	Input offset current—differential pair		0.2	2	μA	V_{CE} = 3V I_C = 1mA
ΔV_{BE1}	Input offset voltage—differential pair		0.35	5	mV	V_{CE} = 3V I_C = 1mA
ΔV_{BE2}	Input offset voltage-isolated transistors		0.45	5	mV	V_{CE} = 3V I_C = 1mA
$\frac{\partial \Delta_{BE}}{\partial T}$	Temperature co-efficient of input offset voltage		2		μV/°C	V_{CE} = 3V I_C = 1mA
$\frac{\partial V_{BE(ON)}}{\partial T}$	Temperature co-efficient of base emitter-voltage		1.8		mV/°C	V_{CE} = 3V I_C = 1mA

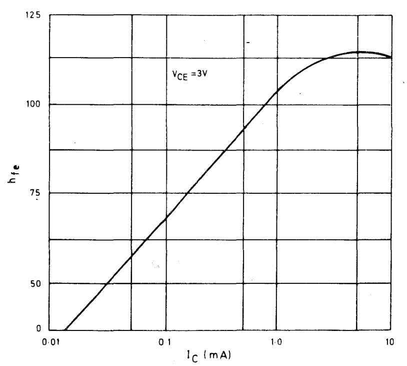
Dynamic Characteristics

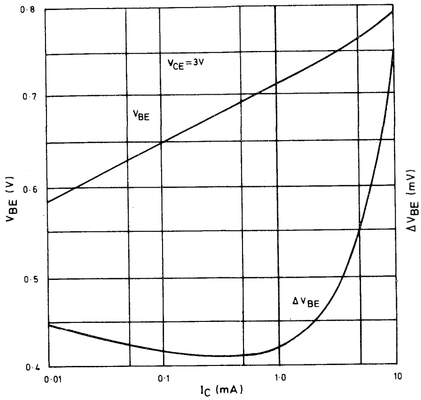
Symbol	Characteristic	Value			Units	Test conditions
		Min.	Typ.	Max.		
N.F.	Wide band noise figure		3.5		dB	f = 10Hz to 10kHz V_{CE} = 3V I_C = 100μA Source resistance = 1kΩ
Y_{fe}	Forward transfer admittance		31–j1.5		mmho	
Y_{ie}	Input admittance		0.3–j0.04		mmho	f = 1MHz
Y_{oe}	Output admittance		0.003+j0.04		mmho	V_{CE} = 3V I_C = 1mA
Y_{re}	Reverse transfer admittance		0.000–j0.003		mmho	
h_{fe}	Forward current transfer ratio		110			
h_{ie}	Short cct. input impedance		3.5		kΩ	f = 1kHz
h_{oe}	Open cct. output admittance		15.6		μmho	V_{CE} = 3V I_C = 1mA
h_{re}	Open circuit reverse voltage transfer ratio		1.8×10^{-4}			
f_t	Gain-bandwidth product	500	600		MHz	V_{CE} = 3V I_C = 3mA
C_{IB}	Emitter-base capacitance		1.7		pF	V_{EB} = 3V I_E = 0
C_{OB}	Collector-base capacitance		1.5		pF	V_{CB} = 3V I_C = 0
C_{CI}	Collector-substrate capacitance		3.0		pF	V_{CS} = 3V I_C = 0

CHARACTERISTIC GRAPHS









ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors. The isolation pin must always be negative with respect to the collectors.

V_{CBO} = 20V V_{EBO} = 15V I_C = 50mA I_B = 25mA
V_{CEO} = 15V V_{CIO} = 20V I_E = 50mA

SL3045C — DG

Storage temperature	—55 °C to +175 °C
Junction temperature	+175 °C
Package dissipation	750mW (derate linearly from 55 °C to +175 °C)

SL3046C — DP

Storage temperature	—55 °C to +125 °C
Junction temperature	+125 °C
Package dissipation	500mW (derate linearly from 55 °C to +125 °C)

PLESSEY SEMICONDUCTORS

SL 3000 SERIES
TRANSISTOR ARRAYS

SL3081D SL3082D

GENERAL PURPOSE HIGH CURRENT NPN TRANSISTOR ARRAYS

The SL3081 and SL3082 consist of seven high current (100mA max) silicon NPN transistors on a common monolithic substrate. The SL3081 is connected in a common emitter configuration and the SL3082 is connected in a common collector configuration.

The SL3081 and SL3082 are capable of directly driving both incandescent seven segment displays and LED seven segment displays.

A separate substrate connection is provided, for maximum flexibility in circuit design.

FEATURES

- Seven Transistors Permit a Wide Range of Applications
- Common Emitter (SL3081) or Common Collector (SL3082) Configuration
- High I_C 100mA max (each transistor)
- Low $V_{CE\ SAT}$ 0.4V Typ. @ 50mA

APPLICATIONS

- Drivers for Incandescent Display Devices
- SL3081: Driver for Common Anode 7-Segment LED Displays
- SL3082: Driver for Common Cathode 7-Segment LED Displays
- MOS Clock and Calculator Display Interface Circuits
- Relay and Solenoid Drivers
- Thyristor and Triac Control Circuitry

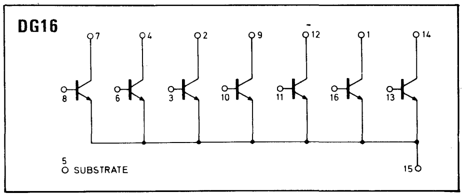


Fig. 1 SL3081 pin connections

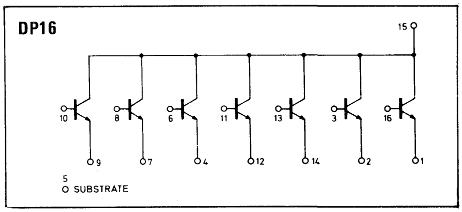


Fig. 2 SL3082 pin connections

ABSOLUTE MAXIMUM RATINGS

$T_A = +25°C$

All electrical ratings apply to individual transistors; termal ratings apply to total package dissipation.

The collector of each transistor of the SL3081 and SL3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and to provide normal transistor operation. To avoid undesired coupling, the substrate (pin 5) should be maintained at either DC or signal (AC) earth.

Electrical Ratings

V_{CEO} = 12V, V_{CBO} = 20V, V_{EBO} = 5V, V_{CIO} = 20V, $I_C = I_E$ = 100mA

Power dissipation 500mW

Thermal Ratings

Storage temperature –55°C to +175°C

Junction operating temperature +175°C

ELECTRICAL CHARACTERISTICS @ $T_A = 22°C \pm 2°C$

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector-base breakdown	BV_{CBO}	20	50		V	$I_C = 500\mu A$, $I_E = 0$
Collector-substrate breakdown	BV_{CIO}	20	70		V	$I_{CI} = 500\mu A$ $I_B = 0$
Collector-emitter breakdown	BV_{CEO}	12	20		V	$I_C = 1mA$, $I_B = 0$
Emitter-base breakdown	BV_{EBO}	5	5.6		V	$I_E = 500\mu A$
DC forward current transfer ratio	h_{FE}	30	68			$V_{CE} = 0.5V$, $I_C = 30mA$
		40	70			$V_{CE} = 0.8V$, $I_C = 50mA$
Collector emitter saturation	$V_{CE(SAT)}$					
SL3081, SL3082			0.27	0.5	V	$I_C = 30mA$, $I_B = 1mA$
SL3081			0.4	0.7	V	$I_C = 50mA$, $I_B = 5mA$
SL3082			0.4	0.8	V	$I_C = 50mA$, $I_B = 5mA$
Collector cut-off current	I_{CEO}			10	μA	$V_{CE} = 10V$, $I_B = 0$
Collector cut-off current	I_{CBO}			1	μA	$V_{CB} = 10V$, $I_E = 0$

PLESSEY SEMICONDUCTORS

SL 3000 SERIES
TRANSISTOR ARRAYS

SL3083D

GENERAL PURPOSE HIGH CURRENT NPN TRANSISTOR ARRAY

The SL3083 is an array of five independent high current (100mA max) NPN transistors on a common monolithic substrate. In addition, two of the transistors (TR1 and TR2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

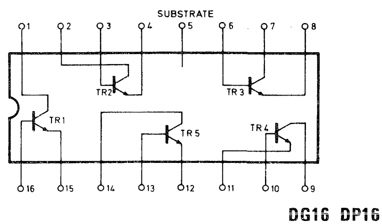


Fig. 1 SL3083 pin connections

FEATURES

- High I_C 100mA Max
- Low V_{CESAT} 0.7V Max @ 50mA
- Matched Pair (TR1 and TR2)
  - ΔV_{BE} ±5mV Max
  - I_{IO} 2.5μA Max @ 1mA
- 5 Independent Transistors plus Separate Substrate Connection

APPLICATIONS

- Signal Processing and Switching Systems Operating From DC to VHF
- Lamp, Relay, Solenoid Driver
- Differential Amplifier
- Temperature Compensated Amplifier
- Thyristor Firing

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C

Electrical Ratings

V_{CEO} = 12V V_{CBO} = 20V, V_{EEO} = 5V, V_{CIO} = 20V, I_C = I_E = 100mA

Power dissipation 500mW

Thermal Ratings

Storage temperature –55°C to +175°C

Junction operating temperature +175°C

All electrical ratings apply to individual transistors; thermal ratings apply to total package dissipation.

The collector of each transistor of the SL3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and to provide normal transistor operation. To avoid undesired coupling, the substrate (pin 5) should be maintained at either DC or signal (AC) earth.

ELECTRICAL CHARACTERISTICS @ T_A = 22°C ±2°C

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Condition
Co' ector-base breakdown	BV_{CBO}	20	50		V	I_C = 100μA, I_E = 0
Collector-emitter breakdown	BV_{CEO}	12	20		V	I_C = 1mA, I_B = 0
Collector-substrate breakdown	BV_{CIO}	20	70		V	I_{CI} = 100μA, I_E = 0 I_B = 0
Emitter-base breakdown	BV_{EBO}	5	5.6		V	I_E = 500μA, I_C = 0
Collector cut off current	I_{CEO}			10	μA	V_{CE} = 10V, I_B = 0
Collector cut off current	I_{CBO}			1	μA	V_{CB} = 10V, I_E = 0
DC forward current transfer ratio	h_{FE}	40	120			V_{CE} = 3V I_C = 10mA
DC forward current transfer ratio	h_{FE}	40	80			V_{CE} = 3V I_C = 50mA
Base emitter voltage	$V_{BE\ (ON)}$	0.65	0.74	0.85	V	V_{CE} = 3V I_C = 10mA
Collector emitter saturation	$V_{CE\ (SAT)}$		0.4	0.7	V	I_C = 50mA, I_B = 5mA
FOR TRANSISTORS T1 AND T2 (As a differential amplifier)						
Input offset voltage	ΔV_{BE}		1.2	5	mV	V_{CE} = 3V
Input offset current	I_{10}		0.7	2.5	μA	I_C = 1mA

PLESSEY
SEMICONDUCTORS

SL3000 SERIES
TRANSISTOR ARRAYS

SL3127C

HIGH FREQUENCY NPN TRANSISTOR ARRAY

The SL3127 consists of five general-purpose silicon NPN transistors on a common substrate. The monolithic construction provides close electrical and thermal matching of the five transistors. Each of the transistors exhibits a low noise figure (3.6 dB typ. @ 60 MHz) and a value of f_T greater than 1.5 GHz. Each of the transistors is individually accessible and a separate substrate connection is provided, which is used to ensure isolation between each transistor.

The SL3127 is pin compatible with RCA CA3127E.

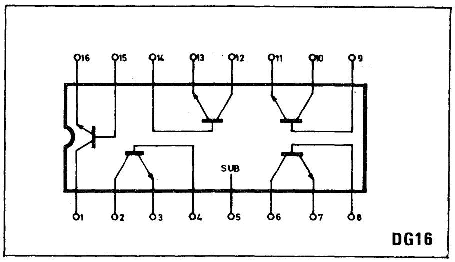


Fig. 1 Pin connections, top view

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Power dissipation	
Any one transistor	150mW
Total package	300mW
Ambient temperature range	
Storage	−55 to +150°C
Operating	−55 to 125°C

The following limiting values apply to each device:

Collector to emitter voltage V_{CEO}	15V
Collector to base voltage V_{CBO}	20V
Collector to substrate V_{CIO}*	20V
Collector current I_C	20mA

*The collector of each transistor is isolated from the substrate by an integral diode. The substrate (pin 5) must be connected to the most negative point in the external circuit to maintain isolation between the transistors.

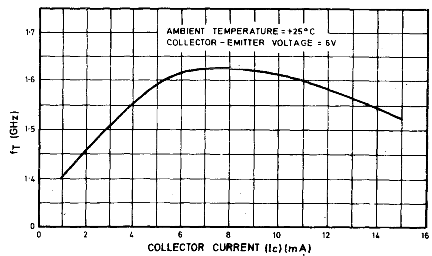


Fig. 2 Typical gain-bandwidth product (f_T) V. collector current

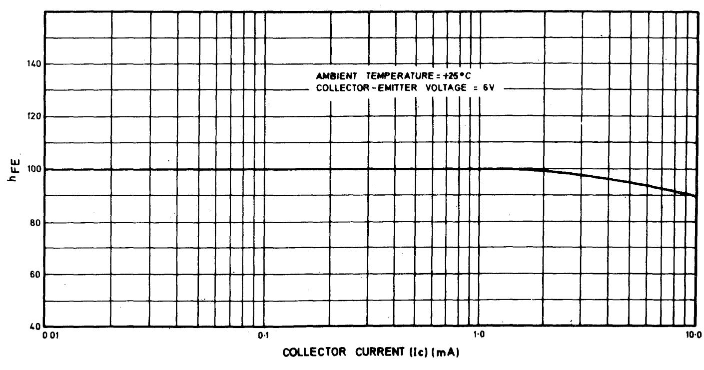


Fig. 3 DC forward current transfer ratio v. collector current

ELECTRICAL CHARACTERISTICS at T_A = +25°C for each transistor

Static characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max		
Collector-base breakdown voltage	BV_{CBO}	20	30		V	I_C = 1μA, I_E = 0
Collector-emitter breakdown voltage	BV_{CEO}	15	18		V	I_C = 1μA, I_B = 0
Collector-substrate breakdown voltage	BV_{CIO}	20	55		V	I_C = 1μA, I_B = 0, I_E = 0
Emitter-base breakdown voltage	BV_{EBO}	4.5	5.5		V	I_E = 10μA, I_C = 0
DC forward current transfer ratio	h_{FE}					V_{CE} = 6V
		40	95			I_C = 5mA
		40	100			I_C = 1mA
		40	100			I_C = 0.1mA
Base-emitter voltage	V_{BE}	0.64	0.74	0.84	V	V_{CE} = 6V, I_C = 1mA
Collector-emitter saturation voltage	$V_{CE(SAT)}$		0.26	0.5	V	I_C = 10mA, I_B = 1mA
Magnitude of difference in V_{BE}	ΔV_{BE}		0.5	5	mV	V_{CE} = 6V, I_C = 1mA
Magnitude of difference in I_B	ΔI_B		0.02	3	μA	V_{CE} = 6V, I_C = 1mA

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Gain-bandwidth product	f_T		1.6		GHz	V_{CE} = 6V, I_C = 5mA
Noise Figure	NF		3.6		dB	V_{CE} = 6V, R_S = 200Ω f = 60MHz, I_C = 2mA
Knee of l/f noise figure curve	–		<1		kHz	V_{CE} = 6V, R_S = 200Ω I_C = 2mA

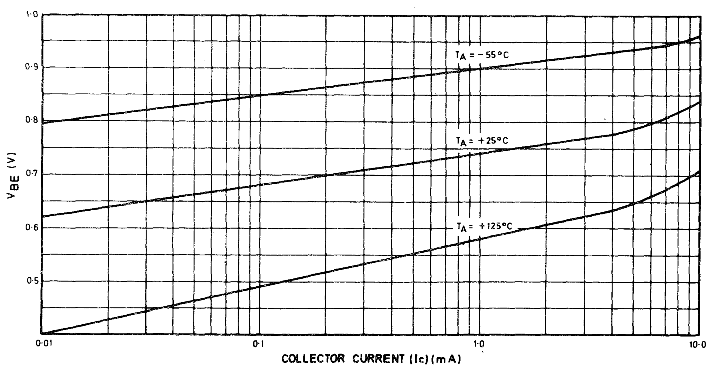


Fig. 4 Base-emitter voltage (V_{BE}) v. collector current

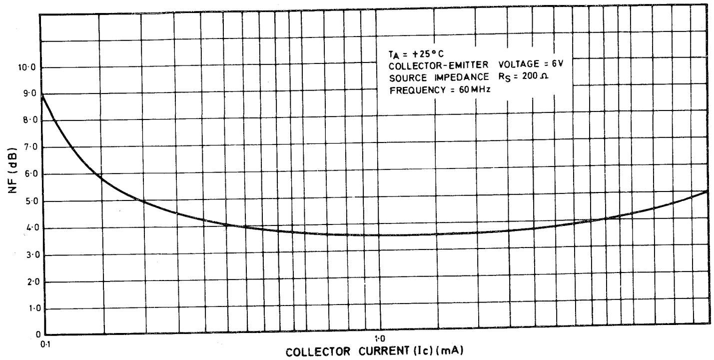


Fig. 5 Noise figure v. collector current

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL3145C
2·5GHz TRANSISTOR ARRAY

The SL3145 is a monolithic array of five general purpose high frequency transistors arranged as a differential pair and three isolated transistors.

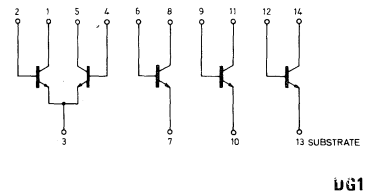


Fig. 1 Schematic and pin diagram

FEATURES

- f_T = 2.5 GHZ
- Wideband Noise Figure = 3dB
- V_{BE} Matching = Better than 5 mV
- Pin-Compatible with SL3045

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} = +25°C ±5°C

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions
Base-Isolation Voltage	10			V	$I_B = 1\mu A$
Emitter-base breakdown	5			V	$I_C = 10\mu A$
Collector-emitter breakdown	8	15		V	$I_C = 10\mu A$
Collector-base breakdown	12	24		V	$I_E = 10\mu A$
Collector-substrate breakdown	20	40		V	$I_C = 10\mu A$
Base-emitter voltage		0.73		V	$V_{CE} = 2V$, $I_C = 1mA$
Static forward current transfer ratio	30	80			$V_{CE} = 2V$, $I_C = 1mA$
Input offset current (differential pair)		0.2	2	μA	$V_{CE} = 2V$, $I_C = 1mA$
Input offset voltage (differential pair)		0.35	5	mV	$V_{CE} = 2V$, $I_C = 1mA$
Input offset voltage (others)		0.45	5	mV	$V_{CE} = 2V$, $I_C = 1mA$
Temperature coefficient input offset voltage		2		$\mu V/°C$	$V_{CE} = 2V$, $I_C = 1mA$
Temperature coefficient base emitter voltage		1.6		mV/°C	$V_{CE} = 2V$, $I_C = 1mA$
Wideband noise figure		3.0		dB	$V_{CE} = 2V$, $I_C = 100\mu A$ $R_S = 1k\Omega$
Gain-Bandwidth product		2.5		GHz	$V_{CE} = 2V$, $I_C = 10mA$
$V_{CE(SAT)}$		0.35		V	$I_C = 10mA$, $I_B = 1mA$
$V_{BE(SAT)}$		0.95		V	$I_C = 10mA$, $I_B = 1mA$
I_{CBO}		0.3		nA	$V_{CB} = 16V$
I_{CIO}		0.6		nA	$V_{CI} = 20V$
I_{BIO}		1.2		nA	$V_{BI} = 10V$
C_{eb}		0.4		pF	Bias = 0V
C_{cb}		0.4		pF	Bias = 0V
C_{cI}		0.8		pF	Bias = 0V

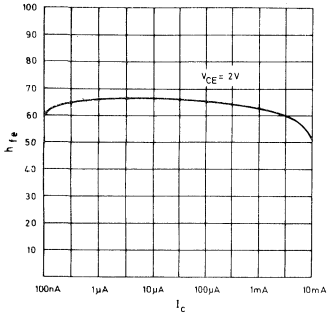


Fig. 2 Typical variation of h_{fe} with I_C

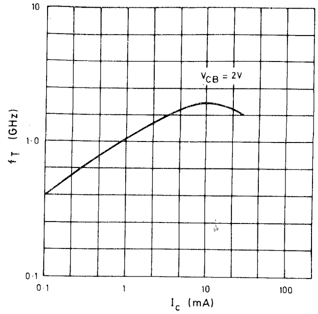


Fig. 3 Typical f_T v. collector current ($f_T = f/h_{fe}$, f = 200MHz)

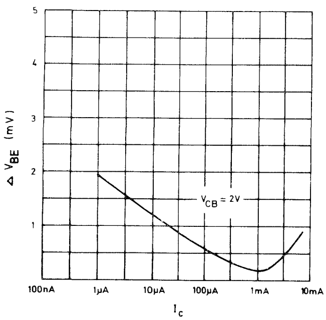


Fig. 4 Typical V_{BE} mismatch v. I_C

ABSOLUTE MAXIMUM RATINGS

Storage temperature: −55°C to +150°C
Junction operating temperature: 150°C
V_{CBO}: 12V V_{EBO}: 5V I_C: 20mA
V_{CEO}: 8V V_{CIO}: 20V
Maximum individual transistor dissipation: 200mW
Total package dissipation: 350mW

PLESSEY
SEMICONDUCTORS

SL 3000 SERIES
TRANSISTOR ARRAYS

SL 3146A, SL 3146C
SL3183A, SL3183C

HIGH VOLTAGE TRANSISTOR ARRAYS

The Plessey Semiconductors SL3146A, SL3146, SL3183A and SL3183 are general-purpose high-voltage silicon NPN transistor arrays on a common monolithic substrate.

SL3146A and SL3146 (high voltage versions of SL3046) each consist of five transistors with two of the transistors connected to form a differential pair. These types are recommended for use in the DC to VHF range. The SL3146A and SL3146 are supplied in either 14 lead plastic DIL package (temperature range −40°C to +85°C) or 14-lead ceramic DIL package (temperature range −55°C to +125°C).

SL3183A and SL3183 consist of five high-current transistors with independent connections for each transistor. In addition, two of these transistors (TR1 and TR2) are matched at low current (i.e. 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. The SL3183A and SL3183 are high-voltage versions of the SL3083 and are supplied in either 16-lead plastic DIL package (temperature range −40°C to +85°C) or 16-lead ceramic package (temperature range −55°C to +125°C).

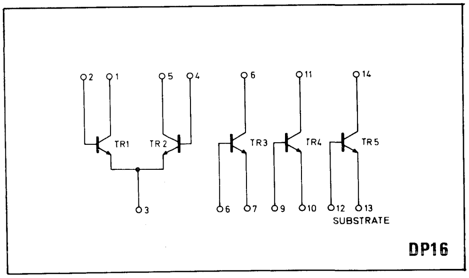


Fig. 1 SL3146/A pin connections

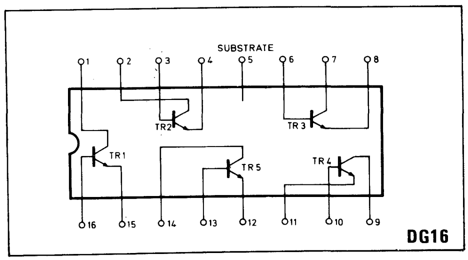


Fig. 2 SL3183/A pin connections

FEATURES

- Matched General Purpose Transistors
- V_{BE} Matched to ±5mV Max.
- Operation from DC to 120MHz (SL3146/A)
- Low Noise Figure: 3.2dB Typ. @ 1kHz (SL3146/A)
- High I_C: 75mA Max. (SL3183/A)

APPLICATIONS

- Signal Processing Systems, DC – VHF
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- Lamp and Relay Drivers (SL3183/A)
- Thyristor Firing (SL3183/A)

ELECTRICAL CHARACTERISTICS @ T_A = +25°C (SL3146/A)

Static Characteristics

Characteristic	Symbol	Value SL3146A Min.	Value SL3146A Typ.	Value SL3146A Max.	Value SL3146C Min.	Value SL3146C Typ.	Value SL3146C Max.	Units	Test Conditions
Collector-base breakdown	BV_{CBO}	50	72		40	72		V	I_C = 10µA, I_E = 0
Collector-emitter breakdown	BV_{CEO}	40	56		30	56		V	I_C = 1mA, I_B = 0
Collector-substrate breakdown	BV_{VIO}	50	72		40	72		V	I_{CI} = 10µA, I_E = 0, I_B = 0
Emitter-base breakdown	BV_{EBO}	5	7.5		5	7.5		V	I_E = 10µA, I_C = 0
Collector cut-off current	I_{CEO}			5			5	µA	V_{CE} = 10V, I_B = 0
Collector cut-off current	I_{CBO}			100			100	nA	V_{CE} = 10V, I_E = 0
DC forward current transfer ratio	h_{FE}		85			85		–	I_C = 10mA
		30	100		30	100		–	I_C = 10µA V_{CE} = 5V
			90			90		–	I_C = 1mA
Base-emitter voltage	$V_{BE(ON)}$	0.63	0.73	0.83	0.63	0.73	0.83	V	V_{CE} = 3V, I_C = 1mA
Collector-emitter saturation	$V_{CE(SAT)}$		0.33			0.33		V	I_C = 10mA, I_B = 1mA
For Transistors TR1 and TR2 (as a Differential Amplifier)									
Input offset voltage	ΔV_{BE}		0.48	0.5		0.48	0.5	mV	V_{CE} = 5V, I_E = 1mA
Base-emitter temperature coefficient	$\frac{\partial V_{BE(ON)}}{\partial T}$		1.9			1.9		mV/°C	V_{CE} = 5V, I_E = 1mA
Input offset voltage temperature coefficient	$\frac{\partial \Delta V_{BE}}{\partial T}$		1.1			1.1		µV/°C	V_{CE} = 5V, I_{C1} = I_{C2} = 1mA
Input offset current	I_{IO}		0.3	2		0.3	2	µA	V_{CE} = 5V, I_{C1} = I_{C2} = 1mA

Dynamic Characteristics

Characteristic	Symbol	SL3146A Min.	SL3146A Typ.	SL3146A Max.	SL3146C Min.	SL3146C Typ.	SL3146C Max.	Units	Test Conditions
Low frequency noise figure	NF		3.25			3.25		dB	f = 1kHz, V_{CE} = 5V, I_C = 100µA, R_S = 1kΩ
Low Frequency Small Signal Equivalent Circuit Characteristics									
Forward current transfer ratio	h_{fe}		100			100		–	
Short-circuit input impedance	h_{ie}		2.7			3.5		kΩ	
Open-circuit output admittance	h_{oe}		15.6			15.6		µmho	f = 1kHz, V_{CE} = 5V, I_C = 1mA
Open-circuit reverse voltage transfer ratio	h_{re}		1.8 x 10^{-4}			1.8 x 10^{-4}		–	
Admittance Characteristics									
Forward transfer admittance	Y_{fe}		31–j1.5			31–j1.5		mmho	
Input admittance	Y_{ie}		0.35+j0.04			0.35+j0.04		mmho	
Output admittance	Y_{oe}		0.001+j0.03			0.001+j0.03		mmho	f = 1MHz, V_{CE} = 5V, I_C = 1mA
Reverse transfer admittance	Y_{re}		0.001–j0.001			0.001–j0.001		mmho	
Gain bandwidth product	f_t	300	500		300	500		MHz	V_{CE} = 5V, I_C = 3mA
Emitter-base capacitance	C_{BE}		0.7			0.7		pF	V_{EB} = 5V, I_E = 0
Collector-base capacitance	C_{OB}		0.37			0.37		pF	V_{CB} = 5V, I_C = 0
Collector-substrate capacitance	C_{C1}		2.2			2.2		pF	V_{CI} = 5V, I_C = 0

ELECTRICAL CHARACTERISTICS @ T_A = +25°C (SL3183/A)

Static Characteristics

Characteristic	Symbol	Value						Units	Conditions
		SL3183A			SL3183C				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
For each transistor									
Collector-base breakdown voltage	BV_{CBO}	50			40			V	$I_C = 100\mu A$, $I_E = 0$
Collector-emitter breakdown voltage	BV_{CEO}	40			30			V	$I_C = 1mA$, $I_B = 0$
Collector-substrate breakdown voltage	BV_{CIO}	50			40			V	$I_{CI} = 100\mu A$, $I_B = 0$, $I_E = 0$
Emitter-base breakdown voltage	BV_{EBO}	5			5			V	$I_E = 500\mu A$, $I_C = 0$
Collector cut-off current	I_{CEO}			10			10	μA	$V_{CE} = 10V$, $I_B = 0$
Collector cut-off current	I_{CBO}			1			1	μA	$V_{CE} = 10V$, $I_E = 0$
DC forward current transfer ratio	h_{FE}	40			40				$V_{CE} = 3V$, $I_C = 10mA$
		40			40				$V_{CE} = 5V$, $I_C = 50mA$
Base-emitter voltage	V_{BE}	0.65	0.75	0.85	0.65	0.75	0.85	V	$V_{CE} = 3V$, $I_C = 10mA$
Collector-emitter saturation voltage	*$V_{CE(SAT)}$		1.7	3.0		1.7	3.0	V	$I_C = 50mA$, $I_B = 5mA$
For transistors TR1 and TR2 (as a differential amplifier)									
Absolute input offset voltage	$\|V_{IO}\|$		0.47	5.0		0.47	5.0	mV	$V_{CE} = 3V$, $I_C = 1mA$
Absolute input offset current	$\|I_{IO}\|$		0.78	2.5		0.78	2.5	μA	$V_{CE} = 3V$, $I_C = 1mA$

*A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

ABSOLUTE MAXIMUM RATINGS @ T_A = 25°C

	SL3146C	SL3146A	SL3183C	SL3183A	
Power dissipation (per transistor)	300	300	500	500	mW
Power dissipation (total package)					
Up to +55°C	750	750	750	750	mW
Above +55°C		Derate linearity 6 - 67			mW/°C
Operating temperature range					
Plastic package	–40 to +85	–40 to +85	–40 to +85	–40 to +85	°C
Ceramic package	–55 to +125	–55 to +125	–55 to +125	–55 to +125	°C
Storage temperature range					
Plastic package	–65 to +150	–65 to +150	–65 to +150	–65 to +150	°C
Ceramic package	–65 to +175	–65 to +175	–65 to +175	–65 to +175	°C
The following ratings apply to individual transistors					
Collector-emitter voltage, V_{CEO}	30	40	30	40	V
Collector-base voltage, V_{CBO}	40	50	40	50	V
Collector-substrate voltage, V_{CIO}	40	50	40	50	V
Emitter-base coltage, V_{EBO}	5	5	5	5	V
Collector current, I_C	50	50	75	75	mA
Base current, I_B			20	20	mA

*The collector of each transistor is isolated from the substrate by an integral diode.

NOTE: The substrate pin must always be negative with respect to the collectors.

PLESSEY
SEMICONDUCTORS

SL78– SERIES
VOLTAGE REGULATORS

SL7800 SERIES

1 Amp THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The SL7800 series of three-terminal positive voltage regulators provides a choice of several fixed output voltages, making them suitable for a wide range of applications. They are particularly useful for local or on-card regulation, thereby eliminating the distribution problems associated with single point regulation.

All the SL7800 series of regulators are available in the TO-3 metal can package. This allows them to deliver over 1A if adequate heat sinking is provided. They also employ internal current limiting, thermal shutdown and output transistor safe area compensation, which makes them essentially blow-out proof.

In addition to being used as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

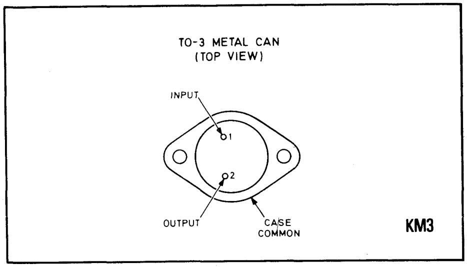


Fig.1 Pin connections

FEATURES

- Output Current in Excess of 1A
- Internal Thermal Overload Protection
- Output Transistor Overload Protection
- Internal Short-Circuit Current Limit
- No External Components Required

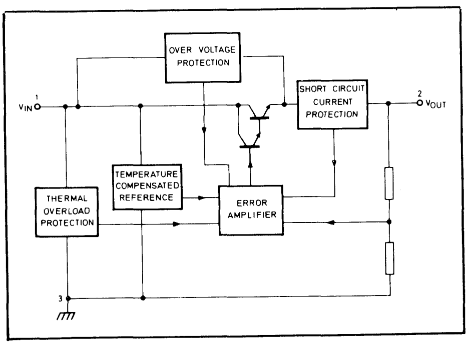


Fig.2 Block diagram

THE SL7800 RANGE	
Type No.	**Nominal Voltage**
SL7805C	5V
SL7806C	6V
SL7808C	8V
SL7812C	12V
SL7815C	15V
SL7818C	18V
SL7824C	24V
SL7830C	30V

ABSOLUTE MAXIMUM RATINGS

Input voltage	
05/06/08/12/15	35V
18/24/30	40V
Internal power dissipation (Note 1)	Internally limited
Storage temperature range	−55°C to +150°C
Operating ambient temperature range	0°C to +70°C
Lead temperature (soldering 10sec time limit)	300°C

Note 1. Typical thermal resistances

Junction-to-case	4°C/W
Junction-to-ambient	35°C/W

ELECTRICAL CHARACTERISTICS

SL7805C

Test conditions (unless otherwise stated):
V_{in} = 10V, I_{out} = 500mA, 0°C ≤ T_J ≤ 125°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Output voltage	4.8	5	5.2	V	T_J = 25°C
Line regulation			100	mV	T_J = 25°C, 7.25V ≤ V_{in} ≤ 25V
Load regulation			100	mV	T_J = 25°C, 5mA ≤ I_{out} ≤ 1.5A
Output voltage	4.75		5.25	V	7.25V ≤ V_{in} ≤ 20V 5mA ≤ I_{out} ≤ 1.0A
Quiescent current		7	10	mA	T_J = 25°C
Quiescent current change with line			1	mA	T_J = 25°C, 8.25V ≤ V_{in} ≤ 25V
Quiescent current change with load			0.5	mA	T_J = 25°C, 5mA ≤ I_{out} ≤ 1.0A
Output noise voltage		40		μV	T_J = 25°C, 10Hz ≤ f ≤ 100kHz
Long term stability			20	mV	
Ripple rejection		62		dB	f = 100Hz, 8V ≤ V_{in} ≤ 18V
Dropout voltage		2		V	T_J = 25°C, I_{out} = 1.0A
Output resistance		20		mΩ	f = 1kHz, T_A = 25°C
Short circuit current		850		mA	T_J = 25°C, V_{in} = 25V
Peak output current		2.1		A	T_J = 25°C

SL7806C

Test conditions (unless otherwise stated):
V_{in} = 11V, I_{out} = 500mA, 0°C ≤ T_J ≤ 125°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Output voltage	5.75	6	6.25	V	T_J = 25°C
Line regulation			120	mV	T_J = 25°C, 8.3V ≤ V_{in} ≤ 25V
Load regulation			120	mV	T_J = 25°C, 5mA ≤ I_{out} ≤ 1.5A
Output voltage	5.7		6.3	V	8.3V ≤ V_{in} ≤ 21V 5mA ≤ I_{out} ≤ 1.0A
Quiescent current		7	10	mA	T_J = 25°C
Quiescent current change with line			1	mA	T_J = 25°C, 9.3V ≤ V_{in} ≤ 25V
Quiescent current change with load			0.5	mA	T_J = 25°C, 5mA ≤ I_{out} ≤ 1.0A
Output noise voltage		45		μV	T_J = 25°C, 10Hz ≤ f ≤ 100kHz
Long term stability			24	mV	
Ripple rejection		59		dB	f = 100Hz, 9V ≤ V_{in} ≤ 19V
Dropout voltage		2		V	T_J = 25°C, I_{out} = 1.0A
Output resistance		20		mΩ	f = 1kHz, T_A = 25°C
Short circuit current		850		mA	T_J = 25°C, V_{in} = 25V
Peak output current		2.1		A	T_J = 25°C

SL7808C

Test conditions (unless otherwise stated):
$V_{in} = 14V$, $I_{out} = 500mA$, $0°C \leqslant T_J \leqslant 125°C$

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Output voltage	7.7	8	8.3	V	$T_J = 25°C$
Line regulation			160	mV	$T_J = 25°C$, $10.5V \leqslant V_{in} \leqslant 25V$
Load regulation			160	mV	$T_J = 25°C$, $5mA \leqslant I_{out} \leqslant 1.5A$
Output voltage	7.6		8.4	V	$10.5V \leqslant V_{in} \leqslant 23V$ $5mA \leqslant I_{out} \leqslant 1.0A$
Quiescent current		7	10	mA	$T_J = 25°C$
Quiescent current change with line			1	mA	$T_J = 25°C$, $11.5V \leqslant V_{in} \leqslant 25V$
Quiescent current change with load			0.5	mA	$T_J = 25°C$, $5mA \leqslant I_{out} \leqslant 1.0A$
Output noise voltage		52		µV	$T_J = 25°C$, $10Hz \leqslant f \leqslant 100 kHz$
Long term stability			32	mV	
Ripple rejection		56		dB	$f = 100Hz$, $11.5V \leqslant V_{in} \leqslant 21.5V$
Dropout voltage		2		V	$T_J = 25°C$, $I_{out} = 1.0A$
Output resistance		20		mΩ	$f = 1kHz$, $T_A = 25°C$
Short circuit current		850		mA	$T_J = 25°C$, $V_{in} = 25V$
Peak output current		2.1		A	$T_J = 25°C$, $V_{in} = 13V$

SL7812C

Test conditions (unless otherwise stated):
$V_{in} = 19V$, $I_{out} = 500mA$, $0°C \leqslant T_J \leqslant 125°C$

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Output voltage	11.5	12	12.5	V	$T_J = 25°C$
Line regulation			240	mV	$T_J = 25°C$, $14.6V \leqslant V_{in} \leqslant 30V$
Load regulation			240	mV	$T_J = 25°C$, $5mA \leqslant I_{out} \leqslant 1.5A$
Output voltage	11.4		12.6	V	$14.6V \leqslant V_{in} \leqslant 27V$ $5mA \leqslant I_{out} \leqslant 1.0A$
Quiescent current		7	10	mA	$T_J = 25°C$
Quiescent current change with line			1	mA	$T_J = 25°C$, $15.6V \leqslant V_{in} \leqslant 30V$
Quiescent current change with load			0.5	mA	$T_J = 25°C$, $5mA \leqslant I_{out} \leqslant 1.0A$
Output noise voltage		75		µV	$T_J = 25°C$, $10Hz \leqslant f \leqslant 100kHz$
Long term stability			48	mV	
Ripple rejection		55		dB	$f = 100Hz$, $15V \leqslant V_{in} \leqslant 25V$
Dropout voltage		2		V	$T_J = 25°C$, $I_{out} = 1.0A$
Output resistance		20		mΩ	$f = 1kHz$, $T_A = 25°C$
Short circuit current		600		mA	$T_J = 25°C$, $V_{in} = 30V$
Peak output current		2.1		A	$T_J = 25°C$, $V_{in} = 17V$

SL7815C

Test conditions (unless otherwise stated):
$V_{in} = 23V$, $I_{out} = 500mA$, $0°C \leq T_J \leq 125°C$

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Output voltage	14.4	15	15.6	V	$T_J = 25°C$
Line regulation			300	mV	$T_J = 25°C$, $17.75V \leq V_{in} \leq 30V$
Load regulation			300	mV	$T_J = 25°C$, $5mA \leq I_{out} \leq 1.5A$
Output voltage	14.25		15.75	V	$17.75V \leq V_{in} \leq 30V$ $5mA \leq I_{out} \leq 1.0A$
Quiescent current		7	10	mA	$T_J = 25°C$
Quiescent current change with line			1	mA	$T_J = 25°C$, $18.75V \leq V_{in} \leq 30V$
Quiescent current change with load			0.5	mA	$T_J = 25°C$, $5mA \leq I_{out} \leq 1.0A$
Output noise voltage		90		µV	$T_J = 25°C$, $10Hz \leq f \leq 100kHz$
Long term stability			60	mV	
Ripple rejection		54		dB	$f = 100Hz$, $18.5V \leq V_{in} \leq 28.5V$
Dropout voltage		2		V	$T_J = 25°C$, $I_{out} = 1.0A$
Output resistance		20		mΩ	$f = 1kHz$, $T_A = 25°C$
Short circuit current		600		mA	$T_J = 25°C$, $V_{in} = 30V$
Peak output current		2.1		A	$T_J = 25°C$, $V_{in} = 20V$

SL7818C

Test conditions (unless otherwise stated):
$V_{in} = 27V$, $I_{out} = 500mA$, $0°C \leq T_J \leq 125°C$

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Output voltage	17.3	18	18.7	V	$T_J = 25°C$
Line regulation			360	mV	$T_J = 25°C$, $21V \leq V_{in} \leq 33V$
Load regulation			360	mV	$T_J = 25°C$, $5mA \leq I_{out} \leq 1.5A$
Output voltage	17.1		18.9	V	$21V \leq V_{in} \leq 33V$ $5mA \leq I_{out} \leq 1.0A$
Quiescent current		7	10	mA	$T_J = 25°C$
Quiescent current change with line			1	mA	$T_J = 25°C$, $22V \leq V_{in} \leq 33V$
Quiescent current change with load			0.5	mA	$T_J = 25°C$, $5mA \leq I_{out} \leq 1.0A$
Output noise voltage		110		µV	$T_J = 25°C$, $10Hz \leq f \leq 100kHz$
Long term stability			72	mV	
Ripple rejection		53		dB	$f = 100 Hz$, $22V \leq V_{in} \leq 32V$
Dropout voltage		2		V	$T_J = 25°C$, $I_{out} = 1.0A$
Output resistance		25		mΩ	$f = 1kHz$, $T_A = 25°C$
Short circuit current		600		mA	$T_J = 25°C$, $V_{in} = 30V$
Peak output current		2.1		A	$T_J = 25°C$, $V_{in} = 23V$

SL7824C

Test conditions (unless otherwise stated):
V_{in} = 33V, I_{out} = 500mA, 0°C ≤ T_J ≤ 125°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Output voltage	23	24	25	V	T_J = 25°C
Line regulation			480	mV	T_J = 25°C, 27.2V ≤ V_{in} ≤ 38V
Load regulation			480	mV	T_J = 25°C, 5mA ≤ I_{out} ≤ 1.5A
Output voltage	22.8		25.2	V	27.2V ≤ V_{in} ≤ 38V 5mA ≤ I_{out} ≤ 1.0A
Quiescent current		7	10	mA	T_J = 25°C
Quiescent current change with line			1	mA	T_J = 25°C, 28.2V ≤ V_{in} ≤ 38V
Quiescent current change with load			0.5	mA	T_J = 25°C, 5mA ≤ I_{out} ≤ 1.0A
Output noise voltage		170		µV	T_J = 25°C, 10Hz ≤ f ≤ 100kHz
Long term stability			96	mV	
Ripple rejection		50		dB	f = 100Hz, 28V ≤ V_{in} ≤ 38V
Dropout voltage		2		V	T_J = 25°C, I_{out} = 1.0A
Output resistance		30		mΩ	f = 1kHz, T_A = 25°C
Short circuit current		275		mA	T_J = 25°C, V_{in} = 35V
Peak output current		2.1		A	T_J = 25°C, V_{in} = 29V

SL7830C

Test conditions (unless otherwise stated):
V_{in} = 40V, I_{out} = 500mA, 0°C ≤ T_J ≤ 125°C

Characteristic	Value			Units	Conditions
	Min	Typ.	Max.		
Output voltage	28.8	30	31.2	V	T_J = 25°C
Line regulation			600	mV	T_J = 25°C, 33.5V ≤ V_{in} ≤ 40V
Load regulation			600	mV	T_J = 25°C, 5mA ≤ I_{out} ≤ 1.5A
Output voltage	28.5		31.5	V	33.5V ≤ V_{in} ≤ 40V 5mA ≤ I_{out} ≤ 1.0A
Quiescent current		7	10	mA	T_J = 25°C
Quiescent current change with line			1	mA	T_J = 25°C, 34.5V ≤ V_{in} ≤ 40V
Quiescent current change with load			0.5	mA	T_J = 25°C, 5mA ≤ I_{out} ≤ 1.0A
Output noise voltage		210		µV	T_J = 25°C, 10Hz ≤ f ≤ 100kHz
Long term stability			120	mV	
Ripple rejection		46		dB	f = 100Hz, 34V ≤ V_{in} ≤ 40V
Dropout voltage		2		V	T_J = 25°C I_{out} = 1.0A
Output resistance		30		mΩ	f = 1kHz, T_A = 25°C
Short circuit current		275		mA	T_J = 25°C, V_{in} = 35V
Peak output current		2.1		A	T_J = 25°C, V_{in} = 35V

TYPICAL APPLICATIONS

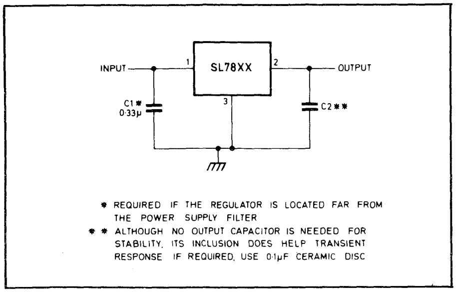


Fig.3 Fixed output regulator

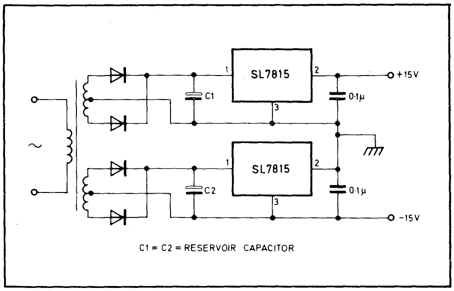


Fig.4 Dual power supply

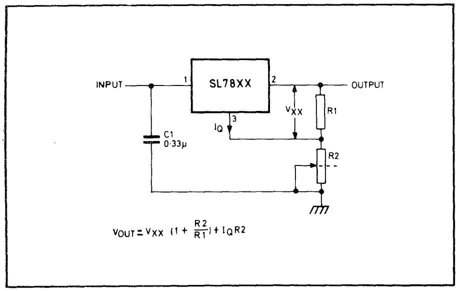


Fig.5 Adjustable output regulator

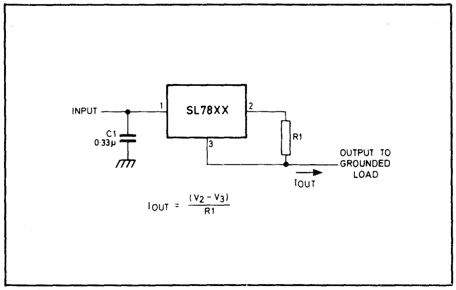


Fig.6 Current regulator

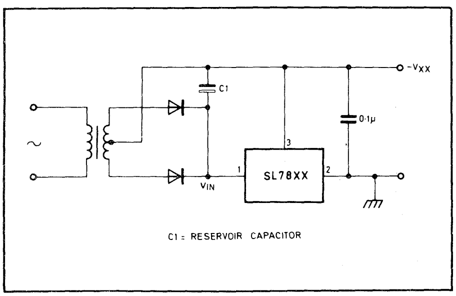


Fig.7 Negative output voltage circuit

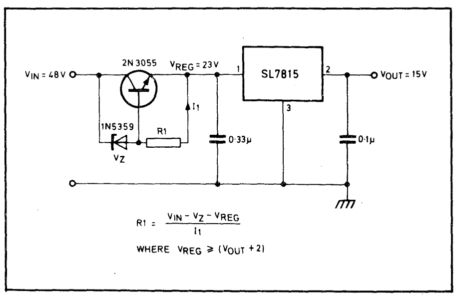
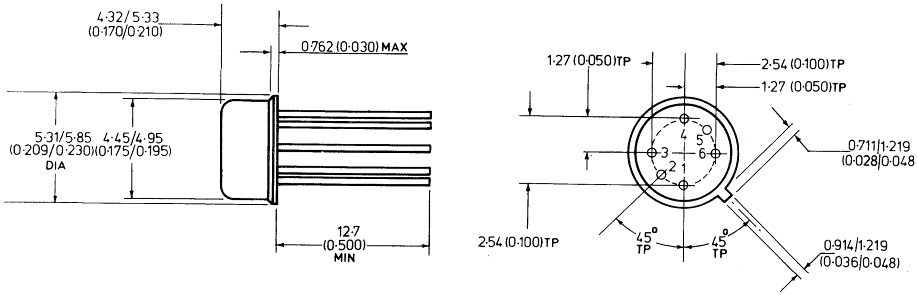


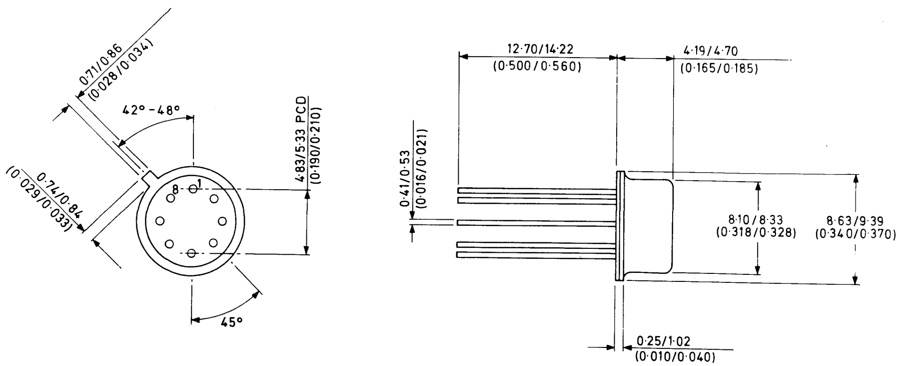
Fig.8 High input voltage regulator

packages



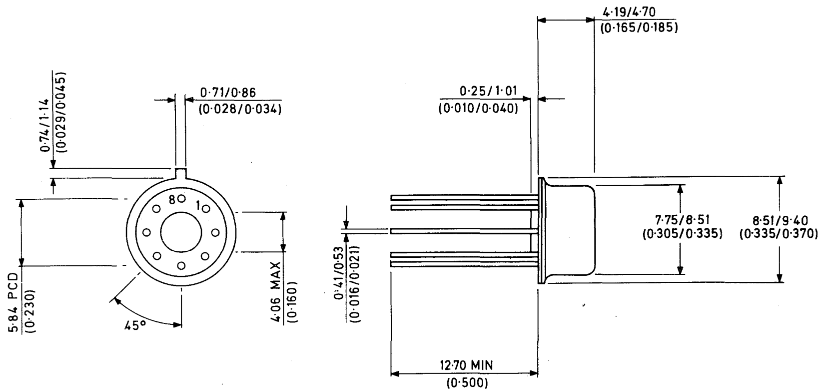
6 LEAD TO-71

CM6



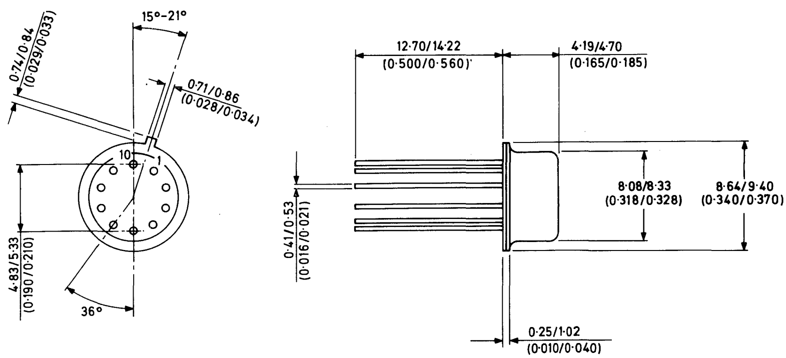
8 LEAD TO-5 (5·08mm PCD)

CM8



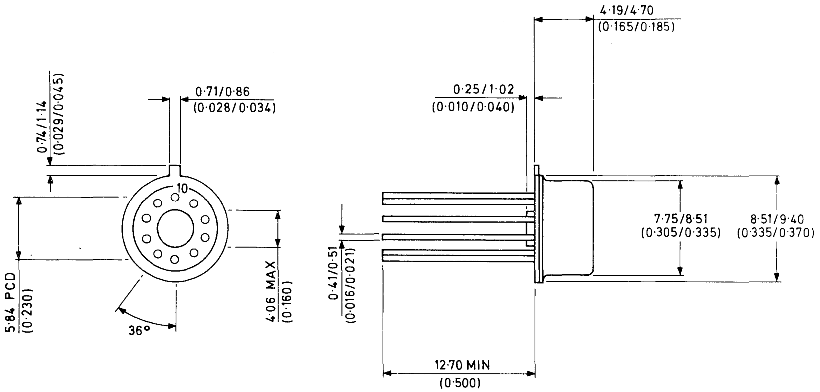
8 LEAD TO-5 (5·84mm PCD) WITH STANDOFF

CM8



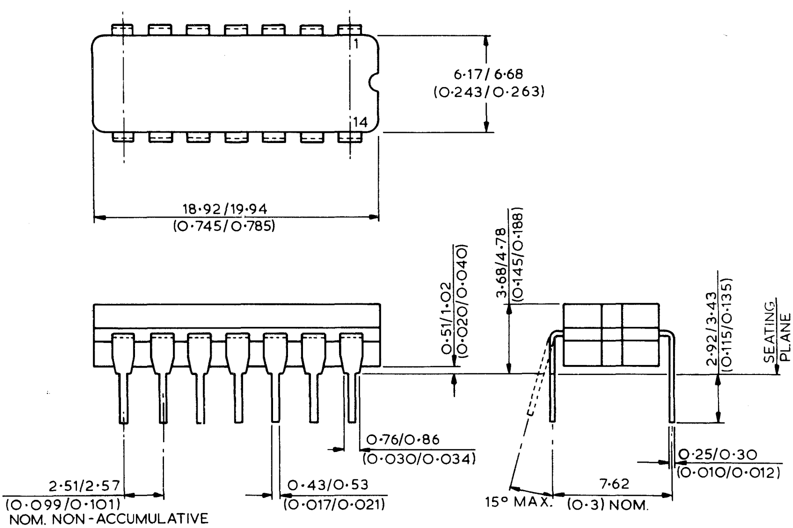
10 LEAD TO-5

CM10



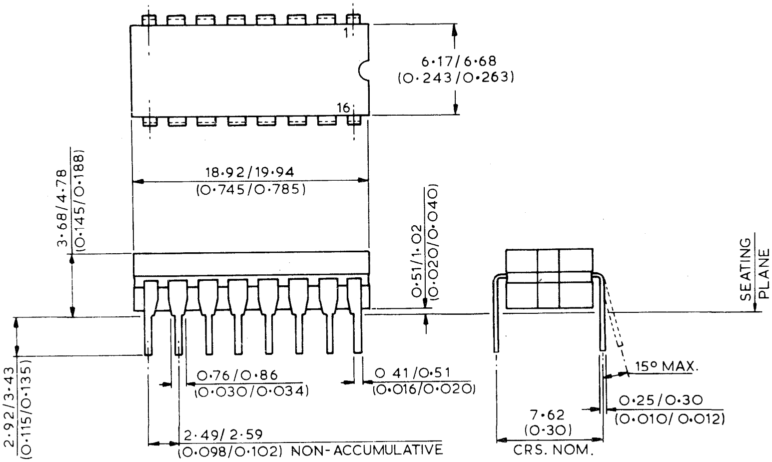
10 LEAD TO-100 (5·84 mm PCD) WITH STANDOFF

CM10



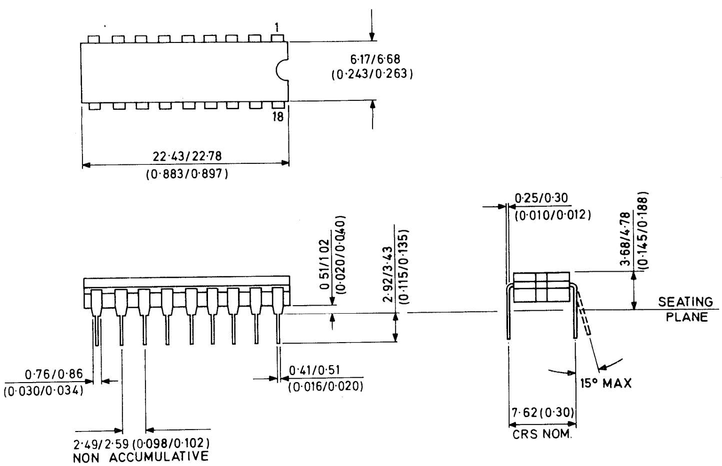
14 LEAD CERAMIC D.I.L.

DG14



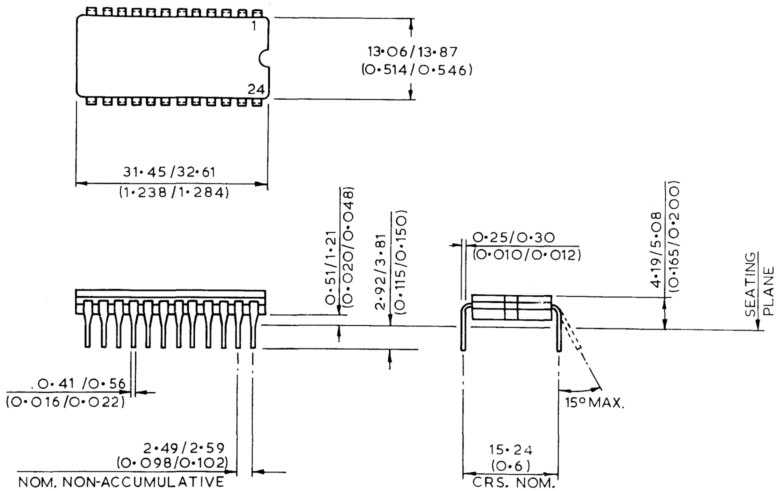
16 LEAD CERAMIC D.I.L.

DG16

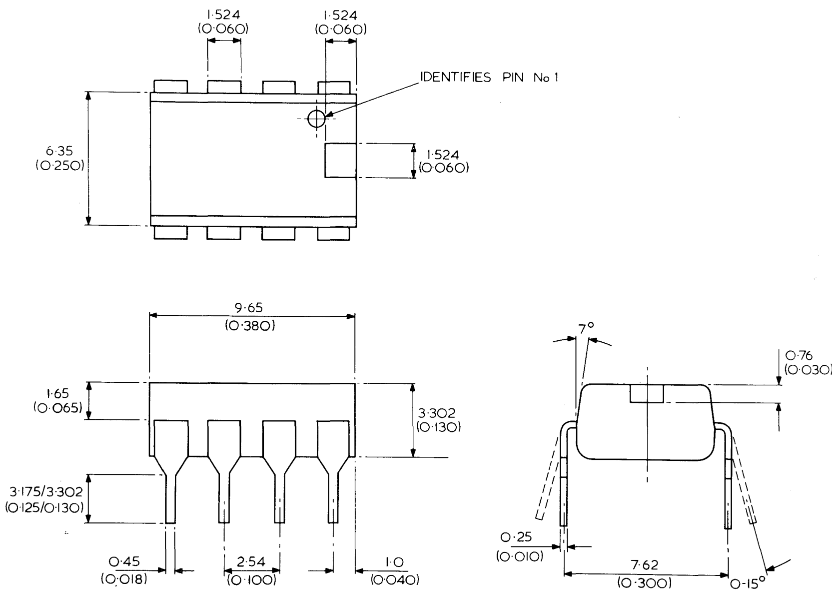


18 LEAD CERAMIC DIL

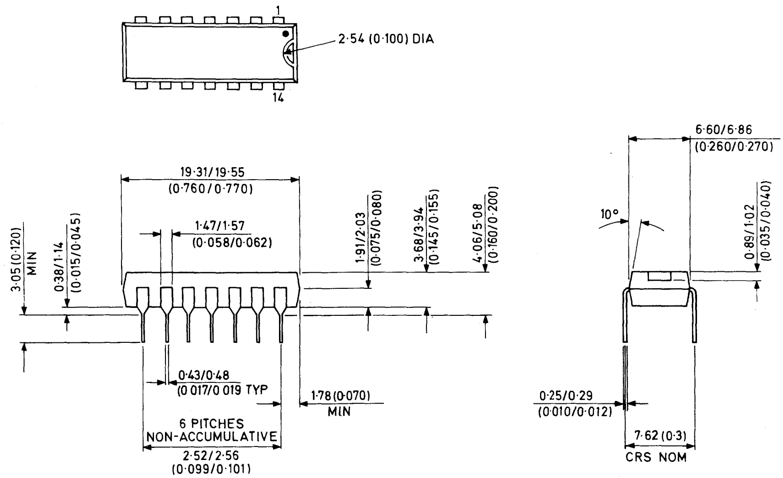
DG18



DG24 24 LEAD CERAMIC D.I.L.

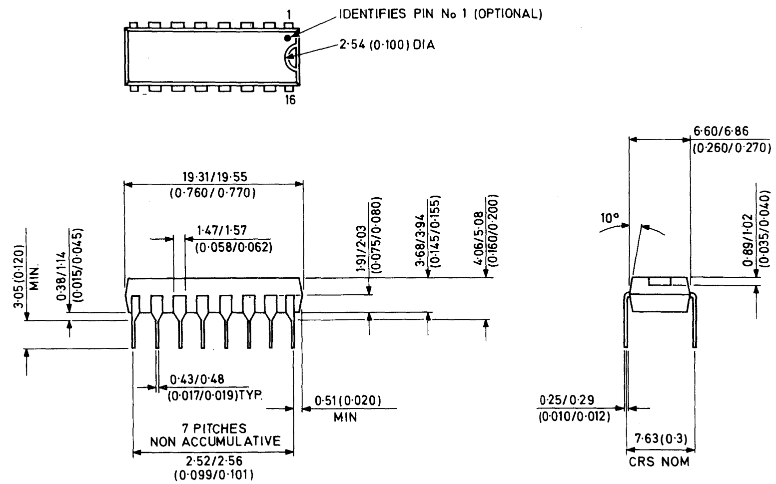


DP8 8 LEAD PLASTIC D.I.L.



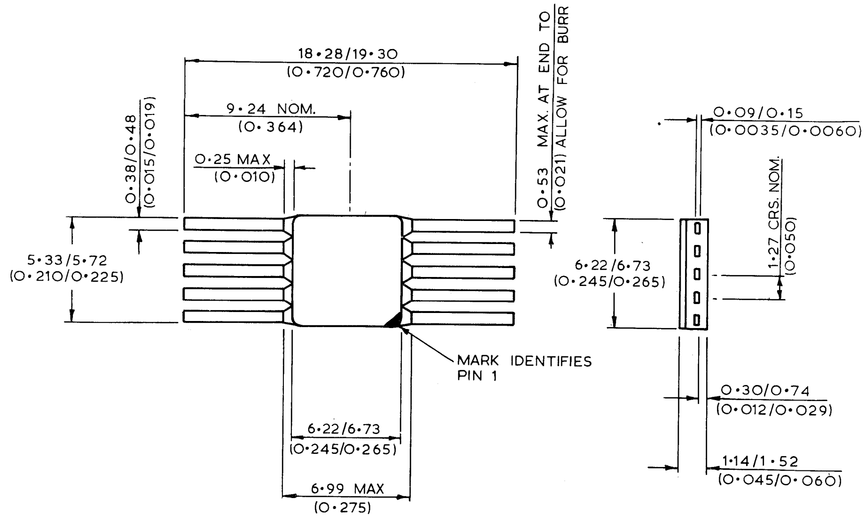
14 LEAD PLASTIC D.I.L.

DP14

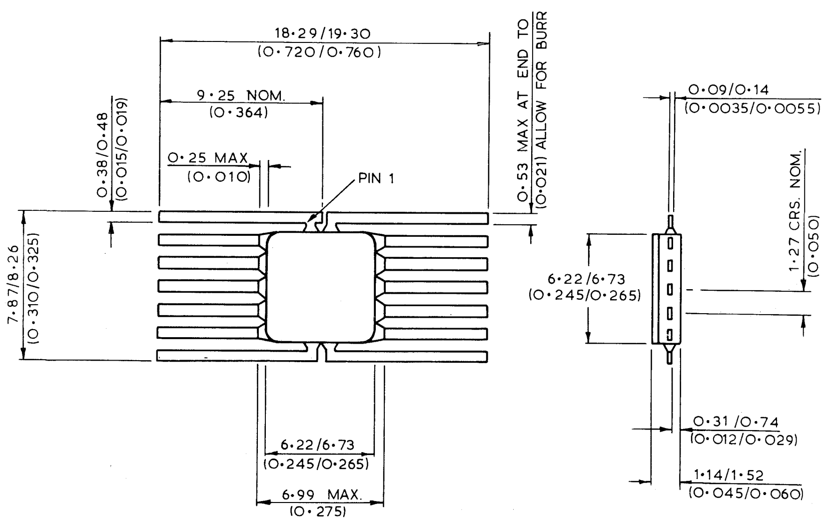


16 LEAD PLASTIC DIL

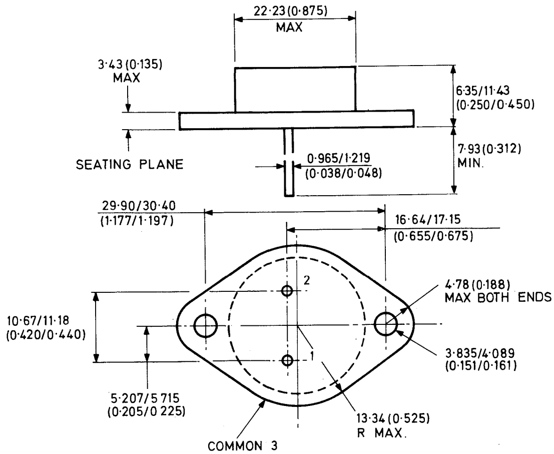
DP16



GM10 10 LEAD FLAT PACK



GM14 14 LEAD FLAT PACK



NOTE : CASE IS THIRD ELECTRICAL CONNECTION

TO–3

KM 3

ordering information

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Swindon
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Tel: (0793) 36251
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PLESSEY SEMICONDUCTORS IC TYPE NUMBERING

Plessey Semiconductors integrated circuits are allocated type numbers which must be used when ordering. The Pro-Electron code is used to identify package outlines.

CM — Multilead TO-5
DG — Ceramic Dual-in-Line (cerdip)
DP — Plastic Dual-in-Line
FM — 10-lead Flatpack
GM — 14-lead Flatpack
KM — Metal TO-3

This package code is for reference purposes only and need only be used when ordering where a device is offered in more than one package style. The package code does not appear on the device itself.

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